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Design and Analysis of Substrate-Integrated Cavity-Backed Antenna Arrays for Ku-Band Applications

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I am submitting herewith a dissertation written by Mohamed Hamed Awida Hassan entitled "Design and Analysis of Substrate-Integrated Cavity-Backed Antenna Arrays for Ku-Band Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Aly E Fathy, Major Professor

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Design and Analysis of Substrate-Integrated Cavity-Backed Antenna Arrays for Ku-Band Applications

A Dissertation
Presented for the
Doctor of Electrical Engineering
Degree
The University of Tennessee, Knoxville

Mohamed Hamed Awida Hassan
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Dedication

To the memory of my father

To my mom, wife and son

Acknowledgement

I would like to express my deep and sincere gratitude to my supervisor, Professor Aly Fathy. His wide knowledge and technical expertise have been of great value for me. In addition, his encouragement, endurance, and understanding have enabled me to overcome all the difficulties I have faced during the past four years and to successfully proceed with my research.

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I owe my loving thanks to my wife Noha El-Bakry, and my son Abd-Elrahman. They have lost a lot due to my research. Without their encouragement and understanding it would have been impossible for me to finish this work. My special gratitude is due to my family in Egypt for their loving support.

Ultimately, I thank God –“And when I am ill, it is He Who cures me”

Abstract

Mobile communication has become an essential part of our daily life. We love the flexibility of wireless cell phones and even accept their lower quality of service when compared to wired links. Similarly, we are looking forward to the day that we can continue watching our favorite TV programs while travelling anywhere and everywhere including satellite channels and the wish list goes on. Mobility, flexibility, and portability are the themes of the next generation communication. Motivated and fascinated by such technology breakthroughs, this effort is geared towards enhancing the quality of wireless services and bringing mobile satellite reception one step closer to the market. On the other hand, phased array antennas are vital components for RADAR applications where the antenna is required to have certain scan capabilities. One of the main concerns in that perspective is how to avoid the potential of scan blindness in the required scan range. Targeting to achieve wideband wide-scan angle phased arrays free from any scan blindness our efforts is also geared.

Conventionally, the key to lower the profile of the antenna is to use planar structures. In that perspective microstrip patch antennas have drawn the attention of antenna engineers since the 1970s due to their attractive features of being low profile, compact size, light weight, and amenable to low-cost PCB fabrication processes. However, patch elements are basically resonating at a single frequency, typically have <2% bandwidth, which is a major deficit in those planar antennas that impedes their usage in relatively wide-band applications regardless of their attractive features. There are various approaches to enhance the patch antennas bandwidth including suspended substrates, multi-stack patches, and metalized cavities backing these patches.

Metalized cavity-backed patch structures have been demonstrated to give the best performance, however, they are very expensive to manufacture. In this dissertation, we develop an alternative low-cost bandwidth enhancement topology. The proposed topology is based on substrate integrated waveguides (SIW). The great potential of this proposed structure lies in being amenable to the conventional PCB fabrication. Moreover, substrate-integrated cavity-backed structure facilitates the design of sophisticated large arrays that were very expensive to develop using the conventional metalized cavity-backed topology, which includes the common broadside arrays used in fixed-beam applications and the scanned phased arrays used in RADAR applications.

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Chapter 1 Introduction

Mobile communication has become an essential part of our daily life. We love the flexibility of wireless cell phones and even accept their lower quality of service when compared to wired links. Similarly, we are looking forward to the day that we can continue watching our favorite TV programs while travelling anywhere and everywhere including satellite channels and the wish list goes on. Mobility, flexibility, and portability are the themes of the next generation communication. Motivated and fascinated by such technology breakthroughs, our satellite antenna group at the University of Tennessee has worked along these lines towards enhancing the quality of wireless services and bringing mobile satellite reception a one step closer to the market.

On the other hand, scan-blindness in phased arrays is the serious problem of having most of the electromagnetic energy reflected back to the feed source at certain scan angle\s. For RADAR applications that would essentially means a blind spot in the scan range where the target will be seriously unseen. Targeting to realize wideband wide-scan angle phased arrays free from any scan blindness our efforts is also directed.

In this dissertation, we investigate the potential of using substrate-integrated waveguide technology in realizing low-cost cavity-backed patch antenna arrays. The great potential of the proposed structures lies in being amenable to the conventional PCB fabrication, which will reflect on a cost reduction of the reception system. Both broadside arrays commonly used in fixed-beam applications and scanned phased arrays typically used in RADAR applications are under exploration. In that perspective, the proposed research work is divided into two main parts. The first part deals with a low cost development of a mobile DBS antenna, and the second part targets the development of a planar phased array antenna. Both applications are based on low-cost SIW cavity-backed patches implementation. Our investigations will be geared towards Ku-band frequency range but it could be easily extended to other frequency bands.

1.1 Background

For satellite reception on the move, the question was not: can we do it or not? It was the possibility of a low profile implementation. Add to that: Is the proposed solution within the customer's anticipated budget? People now can receive satellite signals on the move but they are using bulky reflector antennas, which could explain the limited use/spread of such products [1].

Conventionally, the key to lower the profile of the antenna is to use planar structures. In that perspective microstrip patch antennas have drawn the attention of antenna engineers since the 1970s due

to their attractive features of being low profile, compact size, light weight, and amenable to low-cost PCB fabrication processes [2-3]. However, the inherent limited bandwidth of the microstrip patch antennas is a major deficit in those planar antennas that impedes their usage in relatively wide-band applications regardless of their attractive features [2-4]. Moreover, microstrip phased arrays suffer also from limited scan range due to the existence of surface waves [5-9].

1.1.1 Microstrip Patch Antennas: Design Challenges

1.1.1.1 Limited Bandwidth

Microstrip patch elements are basically resonating at a single frequency, typically have less than 2% bandwidth [2-4], which is a major drawback in their utilization. Generally, the patch's limited bandwidth could be enhanced by either introducing a cavity to back the patch [10-15], or by suspending the patch substrate [16-19].

Cavity-backed patches exhibit superior performance rather than the suspended substrate structures due to their salient features of surface wave suppression, isolation from the surrounding, reduced coupling in an array configuration, better matching and wider scan performance in infinite arrays [12]. However, the conventional cavity-backed patches are usually expensive to manufacture as they require metal casting or CNC machining of the cavity layer.

Recently, SIW technology was elegantly suggested as an alternative technique to facilitate the low-cost implementation of waveguide-like components using a standard PCB technology [20-21]. In principle, the waveguide metal walls could be emulated using via-holes that are properly spaced at approximately $\lambda g/10$ [22], which is similar to previously suggested laminated [23] and post-wall waveguides [24]. Several waveguide-like components were successfully attained using this low-cost SIW fabrication techniques, for example waveguide dividers, directional couplers, waveguide filters, and circulators [25]. SIW has also been successfully used for implementing slotted array antennas [24, 26-28].

Utilization of SIW technology should help in reducing the cost of realizing the cavity-backed antennas. In this dissertation, we extend the use of the SIW cavities to back microstrip patches instead of the conventional metalized ones. The proposed topology is easy to fabricate and should lead to a significant cost reduction.

1.1.1.2 Limited Scan-Range

Generally, the scan blindness phenomenon is likely to appear in planar, cylindrical, or spherical arrays whenever there is a chance of surface wave propagation [29]. In that perspective, the scan-blindness problem is serious in microstrip phased arrays as the surface waves inherently exist in that planar open structure.

In this dissertation, we examine the potential of impeding the surface waves in the microstrip phased arrays by adding SIW cavities to back the radiating patches targeting to resolve both the limited scan range and bandwidth problems while maintaining low cost of fabrication.

1.1.2 **Application I: Mobile DBS Antenna Arrays**

Satellite-communication on the move (SOTM) requirements have put stringent constrains on the radiator occupied space and performance. The antenna is required to be mountable on vans and RVs and should have low profile. Moreover, the antenna is required to be capable of acquiring and tracking a fixed (GEO) satellite while vehicles are stationary or in motion. Meanwhile, the antenna is required to be relatively wideband covering 12.2-12.7 GHz frequency range for the ITU Region 2 (North and South America). On the other hand, from the fabrication point of view it is highly desirable to have a low cost design with a maximum use of automatic assembly. Typical required specification for mobile DBS in USA are given in Table **1.1**, explaining the difficulties/challenges in developing such a product [1].

Table 1.1 Specifications of mobile DBS in USA

Antenna Gain > 32 dB
Antenna Physical Area approx. 240 in² @ 12.45GHz
G/T >12 dB/K
Azimuth Coverage φ=360º
Elevation Coverage 20º<θ<70º from Horizon
Dual Circular Polarization
Low Profile for SUV/VAN/RV for Customers' Satisfaction

*Assuming 60% efficiency (after S. Yang et. al. [1])

Many designs have been proposed till now addressing the current need for this low-cost, low-profile, and highly efficient DBS antenna [14, 18, 28, 30-36]. The proposed antenna topology varies generally between slotted waveguide antenna arrays [28, 30-33, 36] to microstrip patch arrays [14, 18, 35]. A common feature, however, of almost all the proposed solutions is the use of waveguide feed networks for the antenna array to minimize the feed network losses and thus attaining a better antenna.

For example, S. Yang [37] developed a slotted array antenna. It is a low profile substrate integrated waveguide (SIW) array, made of 32 waveguides with 13 slots each as shown in Figure **1.1** . Yang's antenna array efficiently employs a multi-layer printed circuit board technology. The introduction of multi-layer structures has led to considerable size reduction of the overall height of the mobile antenna to

about 3’’ and has rendered a quite low profile structure suitable for mobile DBS reception. The radiating cross-slot elements were etched on the metalized top surface, while a low loss feed structure comprised of SIW elements was similarly printed using the bottom substrate. The top and bottom layers were coupled through transverse slots cut at the interface of the two layers. Meanwhile, the inherent tilted beam of the leaky wave antenna considerably reduced the mechanical steering requirements. Unfortunately, such an antenna could receive only one circularly polarized signal; either LHCP or RHCP one at a time.

Recently Gatti et. al. [36] has also developed a slotted waveguide antenna. But, it is a bidirectional high-performance Ku-band flat antenna for mobile terminals and could be placed on the roof of a double deck train. The developed antenna is based on slotted waveguide structure as shown in Figure **1.2**. The proof-of-concept antenna is conceived by a dielectric-filled slotted waveguide array made of 32 waveguides with 10 slots each, and it is realized in aluminum. Unluckily, this antenna also doesn’t support dual-polarization.

On the other hand, Wang, et. al. presented in [30] a vehicle-mounted satellite antenna for receiving satellite TV while the vehicle is in the move. Their developed antenna is based on a slotted ridged waveguide planar structure. The ridge guide is used to significantly reduce the size of the antenna.

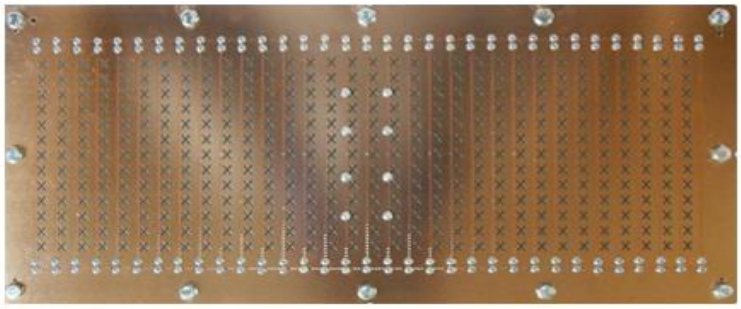


Figure 1.1 Cross-slotted substrate integrated waveguide antenna proposed by S. Yang, et. al. [37].

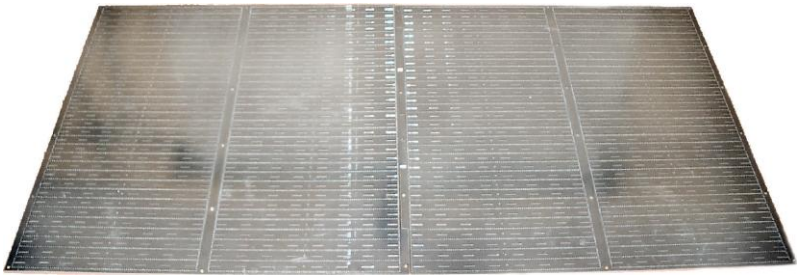


Figure 1.2 Slotted waveguide array for double deck trains developed by Gatti, et. al [36].

The antenna consists of 32 waveguides as shown in Figure **1.3**, with both right-hand circular, RHCP, and left-hand circular polarization, LHCP, output from the opposite ends of the antenna. However, no details were given beyond the presented sketches.

Meanwhile, microstrip patch arrays having a broadside beam were also proposed as potential DBS receiving antennas either with suspended substrate [18, 35], or with cavity-backed patches [14] to enhance the inherent limited bandwidth of the microstrip patches.

For instance, a low-cost quasi-planar Ku-band array of circularly polarized (single polarization) patch antennas on suspended substrate, and benefiting from a low-loss waveguide feed network has been demonstrated by Shahabadi, et. al [18]. The proposed antenna consists of 32 suspended patch elements arranged in a 2-by-16 elements configuration as shown in Figure **1.4**. Waveguide feed network was also used to minimize the feed losses and thus the overall noise temperature at a minimum. The maximum gain of one panel is 23 dBi corresponding to 63% aperture efficiency. However, the structure is relatively complicated in assembly because of the suspended topology. Later, the authors replaced the metalized waveguide feed by an SIW feed in [35].

Alternatively patch antennas were used by Yang et al [14], as well for DBS, but in this case the patches were cavity-backed. A 4x16 cavity-backed patch array shown in Figure **1.5** was proposed and a split-aperture approach was used to achieve the required gain for DBS application while maintaining a low profile. Metalized waveguide feed was again used to lower the feed losses; however single linear polarization has been only demonstrated. Use of a metalized feed guide hindered further development even though it could be easily extended to dual polarization. Meanwhile, the feed thru interconnects using pins to go from the waveguide feed network through the cavity layer to the air and then through the suspended substrate required lots of assembly time and was considered impractical. Further developments of this concept were stopped at this point.

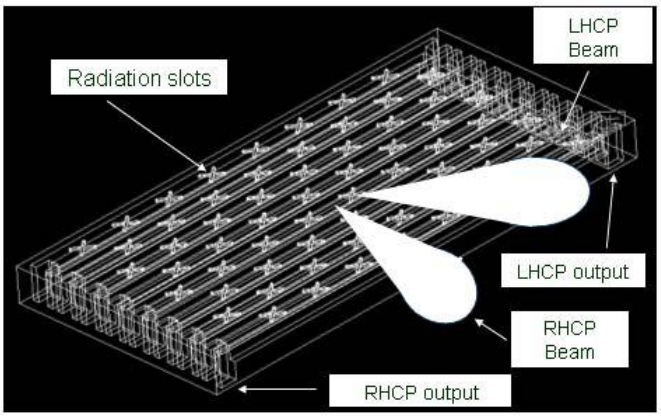


Figure 1.3 Cross-slotted ridged waveguide array developed by Wang, et. al [30].

Obviously, the fabrication of cavity-backed patches is generally expensive, as it would require the integration of metal cavities in the back, necessitating two fabrication processes. The first is the conventional PCB process to print the microstrip patch layer and the second is probably a CNC machining or metal casting process to fabricate the waveguide metalized cavities. The previously prescribed fabrication scenario potentially increases the total fabrication cost and complicates the structure assemblage.

Nevertheless, cavity-backed patches generally exhibit as mentioned before superior performance rather than the suspended substrate structures due to their salient features of surface wave suppression, isolation from the surrounding, reduced coupling in an array configuration, better matching, wider scan performance in infinite arrays, and reduced backward radiation. Therefore, it will be utilized in our subsequent study in developing dual-polarized arrays that could be suitable for DBS applications.

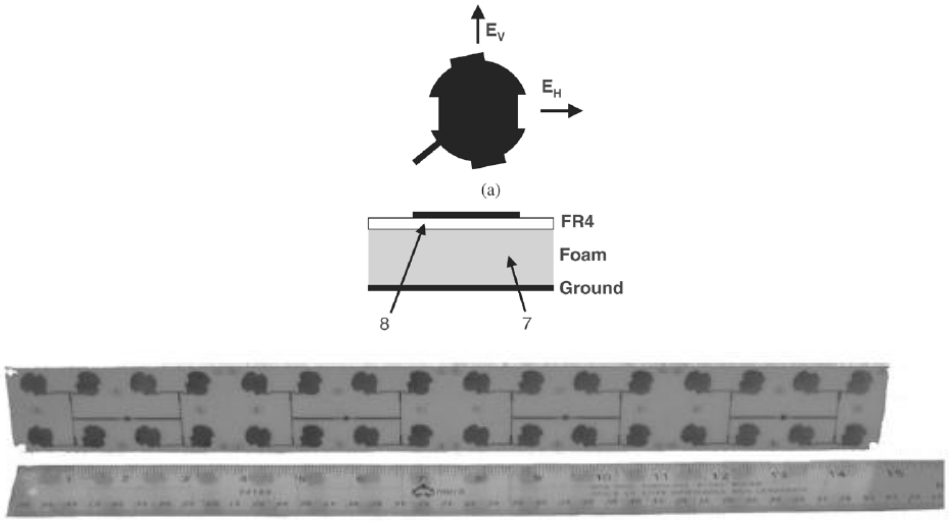


Figure 1.4 Circularly polarized microstrip array developed by Shahdabi, et. al [18].

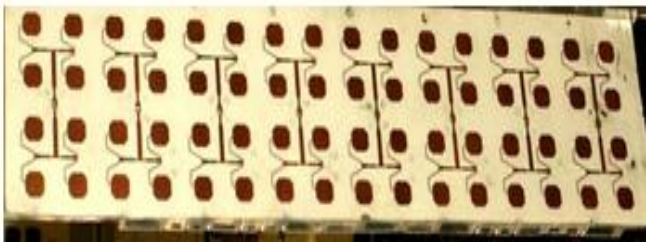


Figure 1.5 Cavity-backed patch array developed by Yang, et. al [14].

Table **1.2** compares the different DBS antenna that have been developed summarizing the features of each one and stressing the advantages and disadvantages of each structure.

Table 1.2 Comparison between the previously developed DBS antennas

	Yang	**Gatti**	**Wang**	**Shahabadi**	**Yang**
Radiating Structure	Slotted Waveguide Array	Slotted Waveguide Array	Slotted Ridged Waveguide Array	Suspended Patch Array	Suspended Cavity-Backed Patch Array
Polarization	LHCP/RHCP	HP/VP	LHCP/RHCP	RHCP	HP
Feed	SIW Feed	SIW Feed	Waveguide	Waveguide	Waveguide
Gain	26.52/26.17 dBi (12.45 GHz)	31.8 dBi (11.575 GHz)	28-32 dBi (12.2-12.7 GHz)	23 dBi (12.45 GHz)	26.5 dBi (12.45 GHz)
Technology	SIW	SIW	Waveguide	Waveguide	Waveguide
Number of layers	Two	Two	One	Three	Three
Advantages	Low Profile	High Gain	Dual Polarization	Good Axial Ratio	High Efficiency
Drawbacks	Single Polarization	Thick Profile, Single Polarization	Thick Profile, Low Efficiency	Single Polarization, Complicated Assembly	Single Polarization

Meanwhile, in summary a comparison between the two basic topologies commonly used for DBS namely; i.e. the slotted waveguide arrays and the microstrip arrays is given in Table **1.3**. Clearly each topology has its own advantages and disadvantages. However, the most critical issue here is the dual-polarization feature which is inevitable for DBS reception in USA. Despite that the slotted waveguide array will render lower profile assuming tilted beam, but it will only acquire single polarization one at a time, unless more complex structures are used like side-by-side ridge guides [30], however that will come on the cost of relatively lower efficiency. That is why the microstrip arrays of broadside beam are more favorable here as they are much easier to fabricate, and can potentially conceive simultaneous dual polarization.

Table 1.3 Slotted waveguide arrays vs. the microstrip patch arrays

	Slotted waveguide array	**Microstrip patch array**
Mounting position	Flat	Inclined at 45 degrees
Required area	Reduced gain by the cosine of the beam squint angle	The beam is always broadside
Beam squint	Serious problem and should be accounted for	No beam squint
Profile	Low	Larger
SIW implementation	Two layers	Three layers
Polarization	Single polarization; one at a time	Simultaneous operation

Based on this decision, the design concerns of the microstrip arrays need to be addressed. First and foremost issue with microstrip designs is their inherent limited bandwidth. As mentioned before, suspended and cavity-backed designs are the common remedies in that perspective. However, despite of the design simplicity of suspended designs its assemblage is usually more complicated. On the other hand cavity-backed designs require multi hybrid fabrication steps to attain both the printed radiating elements and the backing metalized cavities. Therefore we believe that a need exists for a low-cost approach to realize the cavity-backed structures facilitating their utilization in high performance large arrays for both fixed and steered beams applications. The proposed work is geared towards filling that need. In this dissertation, we report on an effective approach to build such low-profile low-cost satellite receiver on the move antenna designed especially for RVs or Mini-Vans utilizing the substrate integrated waveguide technology. This approach potentially should lower the cost of implementation as the whole antenna would be amenable to low-cost printed circuit board (PCB) processes.

1.1.3 **Application II: Scan Blindness Elimination in Microstrip Phased Arrays**

Alongside the DBS antenna application of the cavity-backed microstrip patches discussed in section 1.1.2, we will investigate the use of the SIW cavities instead of metalized cavities in phased arrays of cavity-backed patches.

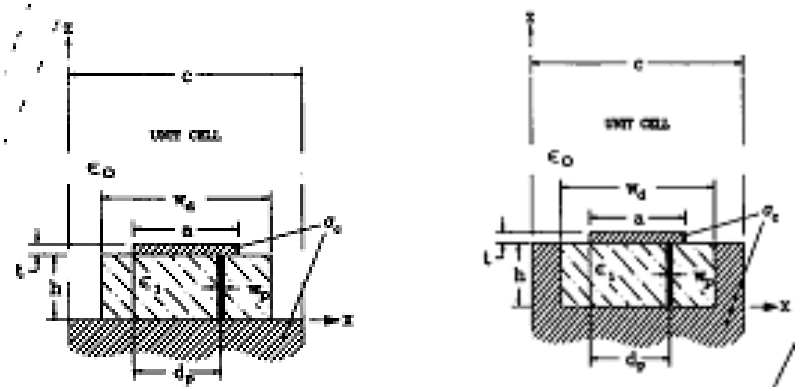
As pointed out before, the scan-blindness in phased arrays is the serious problem of having most of the electromagnetic energy reflected back to the feed source at certain scan angle\s [29]. That scan-blindness problem is very serious in microstrip phased arrays. In fact, the scan blindness severely appears in the relatively thick substrate arrays where the surface waves have more pronounced effects [6, 8]. Using relatively thick substrates however, is needed to increase the fractional bandwidth of the phased array in order to meet the required specifications for certain applications. Therefore, there is always a trade-off between the required impedance bandwidth and scan range in such microstrip phased arrays.

Multiple techniques have been proposed in that perspective in order to eliminate the scan blindness and maintain both wide impedance bandwidth and wide scan range in microstrip phased arrays. The proposed techniques range from substrate modifications [38], using electromagnetic bandgap (EBG) or periodic bandgap (PBG) structures [39-42], employing shorting posts [43-44], using defected ground structures (DGS) [45-46], to adding cavities underneath the radiating elements [10, 47].

Davidovitz, for example, reported in [38] that improved E-plane scanning performance could be achieved upon using arrays that are built on inhomogeneous substrates, as shown in Figure **1.6**. Two types of arrays have been reported. In the first type, the individual strip elements are supported by dielectric slabs of finite extent, as shown in Figure **1.6**(a). In the other type, metallic baffles of substrate-height and

finite width are used to isolate the array elements, as shown in Figure **1.6**(b). The first type was demonstrated on relatively high dielectric constant substrate of ε_r=12.5 and thickness h=0.06λ_0.The method was successful in increasing the E-plane scan range from about 24º to 43º. On the other hand, the second type was demonstrated on a relatively low dielectric constant substrate ε_r=2.5 and thickness h=0.1λ_0, and was successful in increasing the E-plane scan range from about 36º to 57º. Although using substrate modification or baffles has proven useful in obstructing the surface waves, it is usually unrealistic to attain due to the fabrication complexities.

Recently, several researchers have proven the EBG/PBG as an efficient method of surface wave suppression [39-42]. Fu. et. al. in [40], for example, have shown that the (EBG) material, shown in Figure **1.7**, could be utilized in the design of phased arrays of rectangular microstrip patches. The EBGs have been used to surround the radiating elements leading to surface-wave suppression and, therefore, the scan blindness was eliminated. They have numerically demonstrated the topology assuming high dielectric constant substrate of ε_r=10.2 and thickness h=0.06λ_0, and have shown that the E-plane scan range could be enhanced from 30º to 43º upon using the EBG.



(a) (b)

Figure 1.6 Scan blindness elimination by substrate modification developed by Davidovitz [38].

Iluz, et. al. in [42] investigated also the performance of a microstrip antenna phased array embedded in an electromagnetic bandgap substrate. Their results have demonstrated that surrounding the radiating elements by EBGs, shown in Figure **1.8**, could reduce the mutual coupling between elements providing a possible solution to the "blind spots" problem in phased array applications with printed elements. They have experimentally validated the method by building 5x7 array on a high dielectric constant substrate of ε_r=10.2 and thickness h=0.058λ_0 with and without the EBG. Their measured active gain patterns have shown clearly that the scan blindness existed at 30º in the microstrip case has been eliminated upon using the EBG.

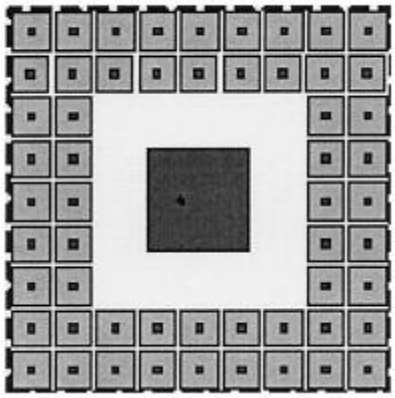


Figure 1.7 Scan blindness elimination by EBG developed by Fu, et. al [40].

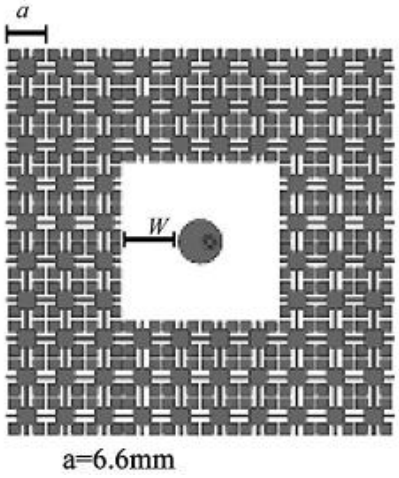


Figure 1.8 Scan blindness elimination by EBG developed by Illuz, et. al [42].

Despite the attractive features of the EBG as an effective surface wave suppression method, it needs significant space on the radiating aperture in order to be integrated around the radiating elements. That is why it works well mostly for relatively high dielectric constant substrates as the miniaturization effect of the substrate is needed in order to stagger both the EBG/PBG and the radiating elements on the substrate (given the space constraints of the unit cell which is typically $0.5\lambda_0$ in order to avoid the grating lobes). However, using high dielectric constant substrate (e.g. ε_r =10.2 as in [40, 42]) will seriously limit the bandwidth of the phased array.

Defected ground structures have also received a considerable attention as a frequency selective surfaces that could be used to absorb the surface waves at certain frequency in the context of scan blindness free phased arrays [45-46]. Hou, et. al. reported in [45] that using the compact H-shaped DGS, shown in Figure **1.9**, the mutual coupling could be reduced between the array elements. That mutual coupling reduction could potentially eliminate the scan blindness in microstrip phased arrays. In their developed array design, the proposed DGS has been inserted between the adjacent E-plane coupled elements to suppress the pronounced surface waves in the E-Plane. They have experimentally validated the potential of the method by measuring the inter-element mutual coupling of two-element array; where the results have shown that a reduction in mutual coupling of 12 dB could be obtained at the operating frequency of the array. The scan properties of the microstrip phased arrays with and without DGS have been numerically demonstrated. Their analysis indicated that the scan blindness of the microstrip phased array built on high dielectric constant substrate of ε_r=10.2 and thickness h=$0.054\lambda_0$ can be significantly eliminated and the E-plane scan range could be enhanced from 40º to 50º.

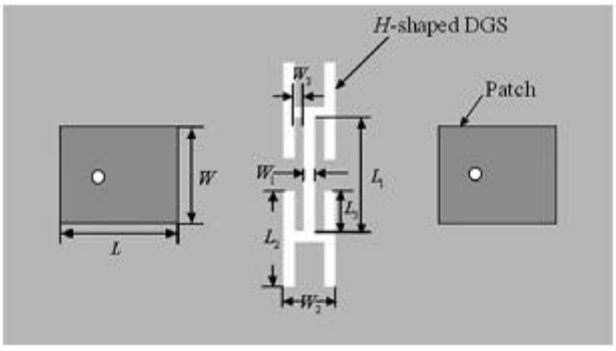


Figure 1.9 Scan blindness elimination by DGS developed by Hou, et. al [45].

However, DGS also have the same space issue of the EBG and it would work mostly for high dielectric constant substrates as the miniaturization effect of the substrate is again needed in order to stagger both the DGS and the radiating elements. Moreover, using DGS will imply also undesired backward radiation.

Meanwhile, using cavities to back the radiating elements, as shown in Figure **1.10**, has been theoretically investigated in [47], and has shown a great potential in eliminating the scan blindness. The utilization of cavities on relatively thick substrates efficiently suppresses the surface waves securing both wide scan performance and wide bandwidth of operation. Zavosh, et. al theoretically demonstrated in [47] that using a low dielectric substrate of ε_r=2.5 and thickness h=0.08λ_0 , a scan range of 85º in the E-plane could be realized with the cavity-backed topology compared to only 48º without the cavity (i.e microstrip case) — a quite an improvement.

However, we face again the realization problem of cavity-backed structures which would typically require a two-step fabrication process; one is the conventional PCB process to print the planar radiating elements and the other is most likely a CNC machining or metal casting processing in order to fabricate the waveguide metalized cavities. That is why not much of experimental results have been reported in the literature about cavity-backed phased arrays. The proposed SIW cavity-backed topology offers a great potential in that perspective.

Table **1.4** summarizes the characteristics and performance of the different phased arrays. Despite that the different techniques have been applied to different substrates of different dielectric constant and thicknesses, we can conclude that the EBG or DGS utilization would likely be possible with relatively high dielectric constant substrates; however that would come at the cost of the bandwidth. On the other hand using substrate modification (baffles) or the cavity-backed techniques on low dielectric constant substrates can secure both wide scan range and wide bandwidth.

In our investigation, we have adopted the use of cavity-backed patches and instead of using metalized cavities like [47], we will use SIW cavities demonstrating similar effects, i.e. its salient features of surface wave suppression, thus eliminating the scan blindness. Implementing SIW instead of solid cavity metal walls has the potential of reducing the weight and lowering the cost.

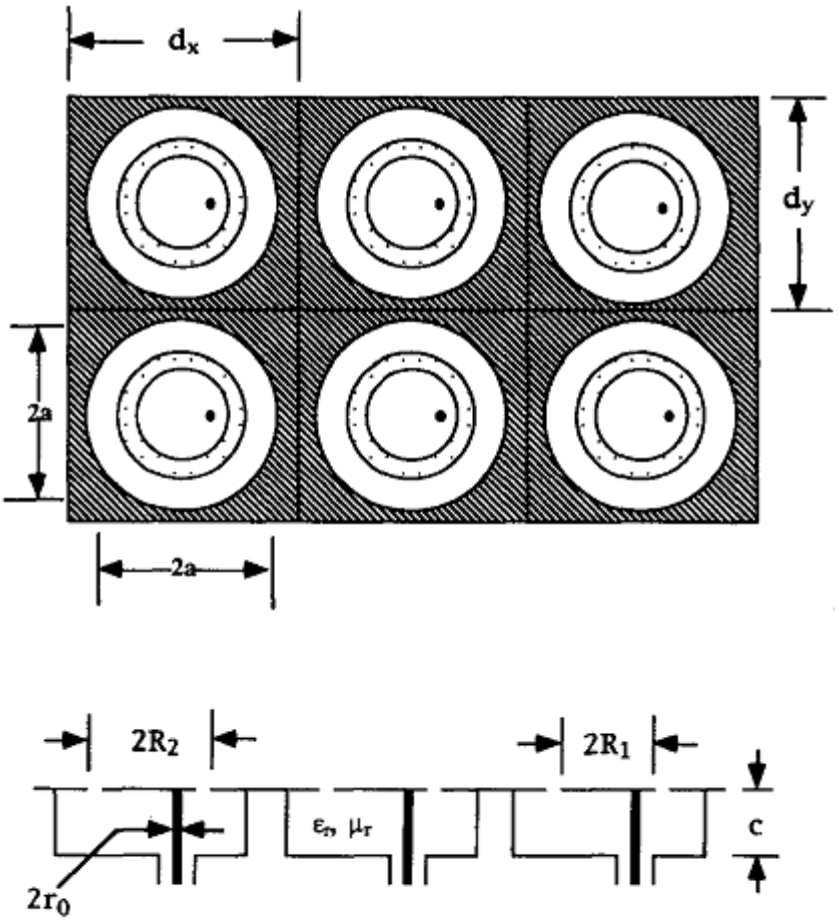


Figure 1.10 Scan blindness elimination by cavity-backing developed by Zavosh, et. al [47].

Table 1.4 Characteristic and performance of the different phased arrays

Used Technique	Substrate	Scan Volume	
		Without	With
Substrate Modification Davidovitz	$h=0.1\lambda_0, \varepsilon_r=2.5$	36º	57º
Cavity-Backed Zafosh, et. al.	$h=0.08\lambda_0, \varepsilon_r=2.5$	48º	85º
EBG Fu, et. al.	$h=0.06\lambda_0, \varepsilon_r=10.2$	30º	43º
EBG Iluvz, et.a l.	$h=0.058\lambda_0, \varepsilon_r=10.2$	Blindness at 30º	No Blindness
DGS Hou, et. al.	$h=0.054\lambda_0, \varepsilon_r=10.2$	40º	50º

1.2 Specific Aims

In this dissertation, the SIW cavity-backed patch antennas will be investigated as a low cost implementation means to develop dual polarized DBS and phased array antennas at Ku-band frequency range. SIW technology will be utilized as a low-cost alternative technology to realize our DBS and phased array antenna implementations. The great potential of the proposed technology lies in being amenable to the conventional PCB fabrication, which will reflect on a significant cost reduction of the reception system.

Specifically, the specific aims of the present research include the following:

1) Investigate the SIW cavity-backed topology as an alternative low-cost approach for dual polarized DBS implementation.
2) Develop a design methodology for large array of cavity-backed patches and its SIW implementation.
3) Study the performance limits of using a microstrip feed network for the DBS antennas.
4) Design and implement dual polarized DBS antennas with waveguide feeds.
5) Investigate SIW technology challenges for stacking more than two layers.
6) Extend the use of SIW technology to fabricate single layer low-cost phased array antennas.
7) Study the probe-fed cavity-backed phased arrays based on a full 2D EM analysis.
8) Carry out a thorough study of probe-fed cavity-backed phased arrays using commercial EM tools.

1.3 Outline of the Dissertation

The dissertation is divided into two main parts. The first part (Chapter 2 to Chapter 5) deals with low-cost development of a mobile DBS antenna and the second part (Chapter 6 and Chapter 7) targets the development of wide-band wide-scan planar phased array antenna. Both parts, however, are based on substrate-integrated waveguide technology (SIW) to realize cavity-backed patch arrays. Our investigations will gear towards Ku-band frequency range but it could be easily extended to other bands.

Chapter 2 investigates alternative set of probe-fed cavity-backed patch antenna topologies. The presented topologies have the potential to widen the inherent limited bandwidth of the conventional microstrip patches from typically 2% to about 15% depending on the height of the backing cavity. The backing cavity acts also effectively to suppress the unwanted surface waves exhibiting superior gain performance of the patch antenna. In the chapter, we will also discuss SIW technology and its implementation in developing cavity-backed patches with a low fabrication cost. Four different structures are investigated corresponding to the different combinations of rectangular or circular patches backed by rectangular or circular SIW cavities. A through comparative study between the four different topologies is presented demonstrating the attractive characteristics of each topology as far as gain, bandwidth, cross-polarization level, and mutual coupling.

Chapter 3 extends the usage of substrate-integrated waveguide (SIW) technology as an alternative low-cost bandwidth enhancement approach in fabricating SIW cavity-backed patch arrays of microstrip feed. The proposed antenna arrays combine the attractive features of the conventional metalized cavity-backed patch arrays like surface wave suppression, high radiation efficiency, and enhanced bandwidth, yet with a low manufacturing cost. A 2x2 SIW cavity-backed sub-array is developed and is used as a basic building block to attain larger arrays of 2x4, 4x4, and 8x8 elements. The design and performance of these arrays are compared to other conventional bandwidth enhancement techniques, which prove SIW as a viable alternative.

Chapter 4 investigates the potential of replacing the conventional microstrip feed used in Chapter 3 by substrate integrated waveguide feed. Three different sized arrays are analyzed and experimentally tested; of 4x4, 4x8 and 4x16 elements. Performance of the arrays is demonstrated and is compared to the corresponding microstrip-fed arrays.

Chapter 5 extends the use of the SIW feed to attain a dual-polarized array suitable for DBS applications. The array is composed of 4x17 elements divided into eight sub-arrays. Each patch is dual-fed by horizontal and vertical microstrip lines. Staggered microstrip dividers are employed to distribute the microwave energy of the two polarizations on the sub-array level while twin SIW 1-8 dividers are

used to distribute the energy to the sub-arrays through a specially designed waveguide to microstrip probe transitions.

Chapter 6 introduces a simplified 2-D numerical analysis to analyze phased arrays of substrate-integrated cavity-backed patches. The analysis is based on Floquet's theorem to solve a 2-D unit cell of the infinite array. The rigorous formulation of the problem yields a Fredholm integral equation. Method of moment is then applied to numerically solve the integral equation. Results would shed light on the potential of using the cavities in widening the scan range of microstrip phased arrays.

Chapter 7 applies the proposed SIW cavity-backed topology in large phased arrays targeting to realize class of wide-band wide-scan microstrip patch phased arrays. The scan performance of the proposed phased arrays is thoroughly investigated varying both the substrate thickness and dielectric constant. Simple design guides lines for the cavity, patch and substrate selection are then presented.

Chapter 8 summarizes the contribution of this work and concludes the dissertation with our recommendations for future relevant research.

Chapter 2 SIW Cavity-Backed Patch Antennas

In this chapter, alternative set of probe-fed cavity-backed patch antenna topologies is investigated. The investigation is geared towards answering some basic design questions like; what is the optimum topology? Should we use circular patches or rectangular ones? Should antenna designers use rectangular backing cavities or circular ones? Can we mix these two shapes?. To address these design issues, four different structures are investigated corresponding to the different combinations of the various circular/rectangular cavity/patch shapes. Meanwhile, for low cost implementation, the substrate-integrated waveguide (SIW) technology is utilized where the cavities are emulated utilizing an array of plated-through via holes. The main characteristics of these antennas including gain, bandwidth, cross-pol level, and mutual coupling are investigated. The study paves the way for utilizing the proposed single-elements in large arrays, which will be addressed in the following chapters.

2.1 Cavity-Backed Patch Antenna

The inherent limited bandwidth of microstrip patch antennas is a major deficit in those planar structures that impedes their usage in relatively wide-band applications regardless of their attractive features of being low-profile, compact size, light weight, and amenable to simplified low-cost fabrication. Extensive research effort therefore, has been dedicated to resolve this serious bandwidth problem. Most of the proposed solution techniques rely on: increasing the volume of the antenna [10-12, 17, 48-54], introducing multiple resonances in the input impedance characteristics of the patch [55-58], or adding lossy material to lower the quality factor, thus enhancing the bandwidth of the microstrip patch antenna [59].

The volumetric approach is relatively the most popular technique compared to the other two techniques due to its potential to enhance the antenna's bandwidth without sacrificing the efficiency of the antenna. Moreover, it is applicable for both single antenna element and antenna arrays in contrast to the other two techniques that are mainly used for the implementation of single element antennas.

In that perspective, several topologies have been proposed to address the bandwidth limitation of microstrip patches by increasing their volume. The simplest topology is to a use a thick substrate, as shown in Figure **2.1**(a), that potentially could enhance the bandwidth to 20% using up to $0.2\lambda_0$-thick substrate (e.g. [48]). However that would seriously degrade the antenna efficiency due to undesired surface wave excitation [3]. Therefore, it is preferred to alternatively use patches that are built with suspended substrates (thus effectively reducing the composite dielectric constant), as shown in Figure

2.1(b) [18, 35], or patches that are backed by cavities, as shown in Figure **2.1**(c) [12, 47], or even a combination of both approaches, as shown in Figure **2.1**(d) [60], to minimize surface wave excitation and its associated losses by reducing the dielectric loading while achieving a wider operating bandwidth by increasing the volume under the radiating patch.

Suspended substrate designs generally are more common for the ease of their manufacturability. On the other hand, the fabrication of the cavity-backed patches is not as common, as it would require the integration of metal cavities in the back -- requiring two fabrication processes. Nonetheless, cavity-backed patches exhibit superior performance when compared to suspended substrate structures due to their significant surface wave suppression, reduced coupling, better matching, and wider scan performance in an infinite array environment [12, 47].

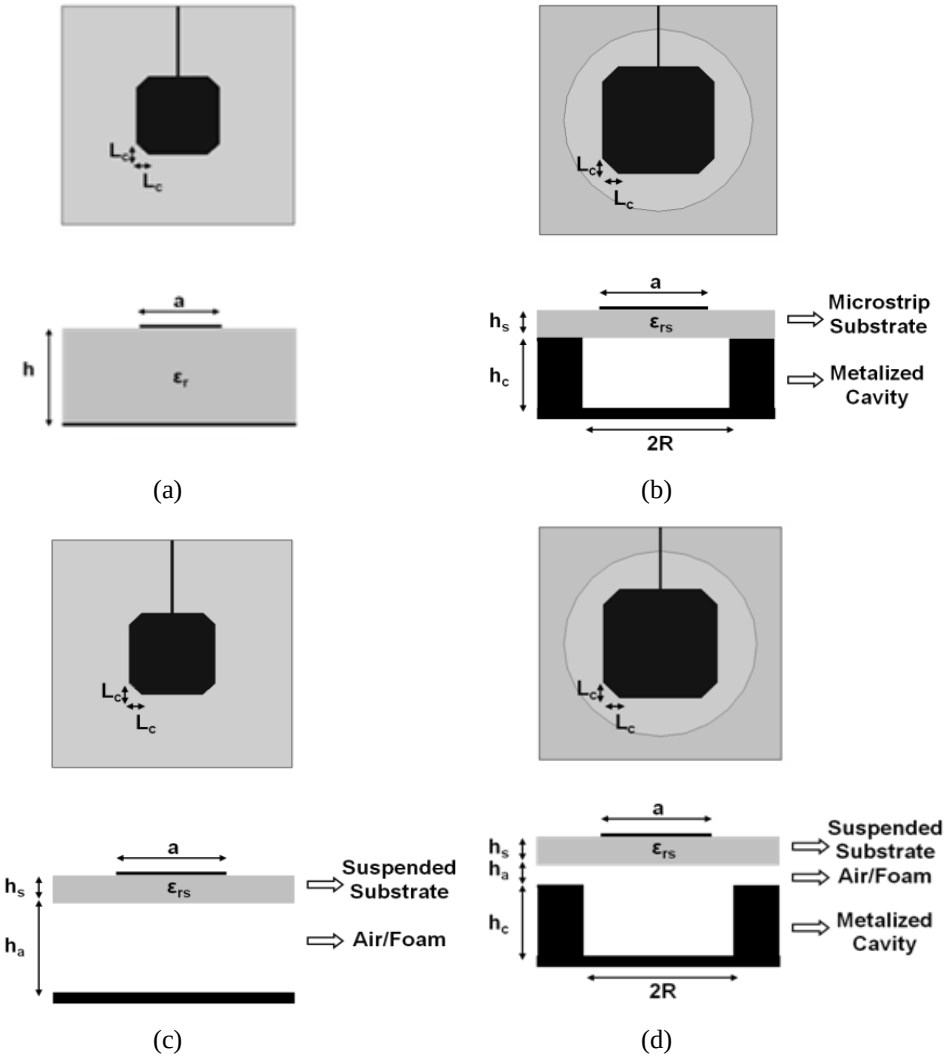


Figure 2.1 Conventional bandwidth enhancement techniques. (a) Microstrip patch on thick substrate. (b) Cavity-backed patch. (c) Suspended patch. (d) Cavity-backed suspended patch.

Table **2.1** compares the performance of the conventional bandwidth enhancement techniques showing the limitation of each method. It clearly shows the advantages of the cavity-backed patch approach which has the best performance, however their expensive fabrication cost typically hinders their usage in many applications. Therfore, finding a low-cost approach to realize the cavity-backed structures will pave the way for their relaization. Substrate-integrated waveguide technology is an appropriate key in that prespective. In the following section, we will highlight the SIW technology first, then we will present a design reciepe for utilizing the SIW in building four distinct topologies of cavity-backed patches.

Table 2.1 Performance comparison of the different bandwidth enhancement techniques

	Aperture Efficiency	Fabrication Cost	Assemblage
Thick Microstrip Patch	Poor	Low	Easy
Suspended Patch	Good	Fair	Complicated
Metalized Cavity-Backed Patch	Best	Expensive	Complicated
Cavity-Backed Suspended Patch	Good	Expensive	Complicated

2.2 SIW Technology

Recently, SIW technology was suggested by Professor Ke Wu's group at the University of Montreal as an alternative technology to facilitate a low-cost implementation of waveguide-like components using the standard PCB fabrication process [21]. SIW technology makes it feasible to integrate both planar circuitry (microstrips, feed transitions, etc …), and 3-D waveguide components (waveguide lines, dividers, etc …) in a single structure that could be easily fabricated with a high precision in a planar form using a standard printed circuit board or other planar processing techniques [22]. These printed circuit fabrication techniques can achieve very fine (precise) circuit dimensions using chemical etching at a fraction of the cost of the alternative bulky waveguide components that are typically fabricated using precise mechanical processing; like numerically controlled machinery.

In principle, the waveguide metal walls could be emulated using via-holes that are properly spaced at approximately $\lambda_g/10$, as shown in Figure **2.2**, which is similar to the laminated waveguides previously

suggested by Uchimura, et. al. in 1998 [23], or the post-wall waveguide that were also previously proposed by Hirokawa, et. al in 1998 [24]. Ke Wu and his group, however, worked effectively to further enhance the proposed SIW technique after re-introducing it in 2003 [21].

Several waveguide-like components were successfully demonstrated by Ke Wu's group and others, using this low-cost SIW fabrication technique. For example waveguide dividers, directional couplers, waveguide filters, and circulators [25] have been designed and presented. SIW has been also successfully used for implementing slotted array antennas [24, 26-28] to minimize feed losses.

Using SIW, fortunately, should surmount the hurdle of fabricating these cavity-backed patches. Prior implementation of cavity-backed patches required the use of conventional PCB process to print the microstrip patch layer and either CNC machining or metal casting process to fabricate the waveguide metalized cavities. Alternatively, here SIW cavity-backed patches would be amenable to only one PCB fabrication process; thus eliminating the relatively expensive machining or casting step.

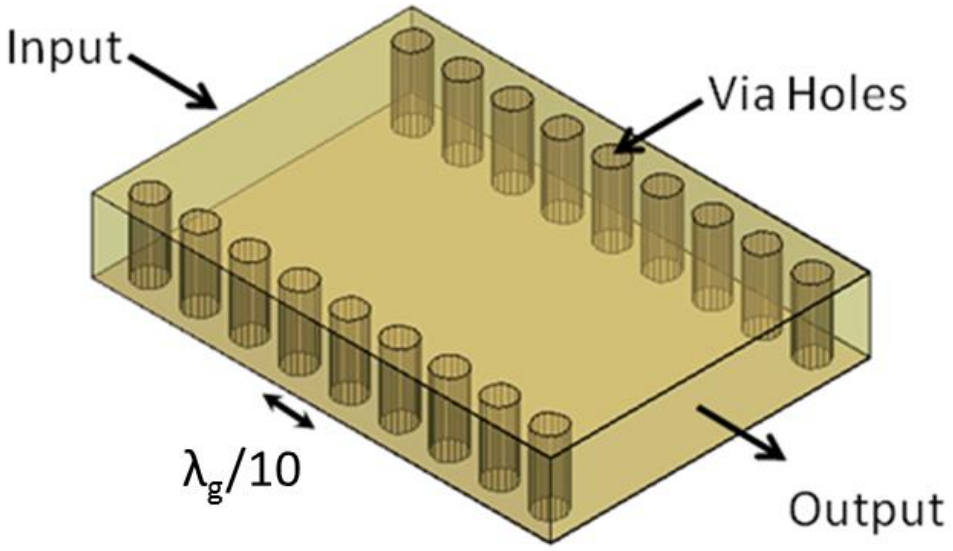


Figure 2.2 Substrate-integrated waveguide (SIW).

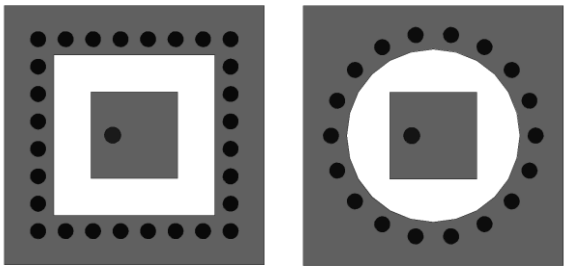
2.3 SIW Cavity-Backed Microstrip Patch Antenna Configuration

Figure **2.3** shows the four different proposed topologies of the probe-fed SIW cavity-backed patch antennas. These four different proposed shaped elements are simply implemented using a single substrate of dielectric constant ε_r and a height h. A rectangular/circular patch of side length/diameter $2a$ is printed on the top conductor layer of the substrate and is fed through a probe. Meanwhile, the top conductor layer has a rectangular /circular opening of side length/diameter $2R$ around the patch. Many via holes spaced along that rectangular/circular opening are drilled in the substrate and are then through-platted constituting the SIW rectangular cavity backing the radiating element (patch surrounded by a slot). Here thereafter we will refer to the different shaped elements by the acronym "Rec-Rec", "Rec-Cir" corresponding to the rectangular patch backed by rectangular or circular cavity structure, as shown in Figure **2.3**(a) and (b), respectively and "Cir-Cir", "Cir-Rec" corresponding to the circular patch backed by circular or rectangular cavity structure, as shown in Figure **2.3**(c) and (d), respectively.

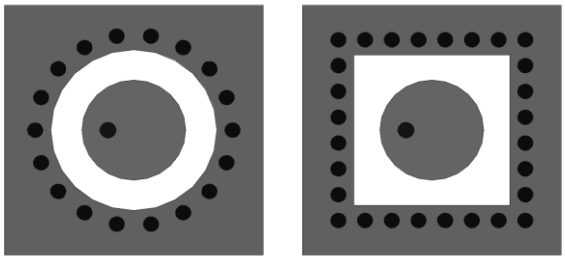
Before going to the design details of the SIW cavity-backed antennas, the SIW cavities have leakage loss and in order to evaluate such loss we will first consider them as resonating structures to investigate their leakage characteristics.

2.4 SIW Cavities

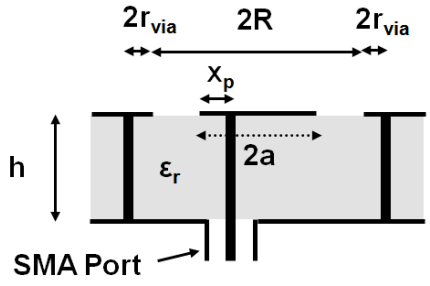
In fact, the main role of a cavity that is backing the patch antenna is to effectively suppress the parasitic surface waves propagation, thus confining the energy underneath the patch. However, the usage of SIW cavities instead of solid wall ones can cause some leakage and reduce the effectiveness of surface wave suppression. In that perspective, it is imperative to study the leakage characteristics of these SIW cavities. Hence, we first investigate the design issues relevant to the SIW cavity implementation; which include the effect of via holes' diameter and spacing so that we can identify the most critical and practical design parameters in minimizing their leakage loss. Second, we will set equivalence between the emulated SIW cavity and its solid wall corresponding one, as shown in Figure **2.4**. Such equivalence was previously developed for propagating waveguide structures [20, 22, 61-62], however here we extend this equivalence to cavities as well, upon taking the resonance nature of the structure in hand into account. Such equivalence would be very useful for large arrays where the computational time could be drastically reduced, upon replacing the SIW cavities by their equivalent solid wall ones, assuming a very low mutual coupling between the elements (as a first order approximation). However, definitely for more accurate results it could require simulating the SIW walls as well to account for such coupling.



(a) (b)



(c) (d)



(e)

Figure 2.3 Proposed probe-fed SIW cavity-backed microstrip patch antennas. (a) Rectangular patch backed by rectangular cavity "Rec-Rec". (b) Rectangular patch backed by circular cavity "Rec-Cir". (c) Circular patch backed by circular cavity "Cir-Cir". (d) Circular patch backed by rectangular cavity "Cir-Rec". (e) Side view, where r_{via} is the via holes radius.

In our investigation here, we have used a 3-D electromagnetic simulation tool "HFSS" [63], where we have modeled both the rectangular and circular SIW cavities in a transmission setup such that the cavity is excited at the input and output sides by coaxial probes (with minimal cavity perturbation due to coaxial probes penetration), as shown in Figure **2.4**(c). To isolate the leakage loss from the conductor and dielectric losses, we have assumed in our model perfect electric conductors and zero loss dielectric substrates. Subsequently, we have run an extensive parametric study varying both the diameter and spacing in steps and have numerically calculated the S-parameters while monitoring both S_{11} and S_{12} to estimate the leakage loss at resonance; which is given by

$$L_{leakage} = -10 \cdot \log_{10}\left(\left(S_{11}\right)^2 + \left(S_{12}\right)^2\right) \tag{2-1}$$

Meanwhile, we have defined an equivalence parameter "P_{eq}" as

$$P_{eq} = \frac{R_{cavity}}{R_{SIW}} \tag{2-2}$$

Where R_{SIW} , and R_{cavity} are the radii of the SIW and the equivalent solid wall cavities resonating at the same frequency. Despite that the radii of the solid wall rectangular/circular cavities could be explicitly calculated given the required resonance frequency, here we resorted to the same simulation setup, shown in Figure **2.4**(c) to calculate it, in order to account for its termination loading effects. (For example, in case of a rectangular cavity with ε_r =2.2, h=1.57 mm, and $2R_{cavity}$=15.56 mm, the termination loading effect causes the TM_{110} resonance frequency to shift from 9.1915 GHz to 9.39 GHz corresponding to about 2.2% frequency shift).

Figure **2.5** demonstrates the characteristics of a rectangular SIW cavity that are presented by contour plots for the calculated equivalence parameter "P_{eq}" in Figure **2.5**(a) vs. the via holes' spacing and diameter normalized to the resonant wavelength of the cavity. It is interesting to note that P_{eq} ranges from 0.91 in case of densely spaced relatively large via holes to 1.04 in case of sparsely spaced relatively small via holes. Meanwhile, Figure **2.5**(b) shows a contour plot for the leakage loss in dB. Subsequently, it is essential to select via holes' diameter and spacing that minimize the leakage loss. In that perspective, we have chosen a 0.1 dB loss as an adequate margin for the leakage loss and marked the area which is in compliance within this condition, as shown in Figure **2.5**(b).

Similarly, the equivalence parameter and leakage loss of the circular SIW cavity are indicated in Figure **2.6**. In this case, P_{eq} ranges from 0.93 in case of densely spaced relatively large via holes to 1.05 in case of sparsely spaced relatively small via holes, as shown in Figure **2.6**(a), while the region of interest where the leakage loss is less than 0.1 dB is again marked in Figure **2.6**(b).

Based on the aforementioned analysis, we have implemented the SIW cavities to be used in the cavity-backed patch antennas with via holes of 0.059 λ_r in diameter with a linear spacing of 0.14 λ_r for the rectangular shaped, while the vias holes are of 0.066 λ_r in diameter with an angular spacing of 0.145 λ_r for the circular ones.

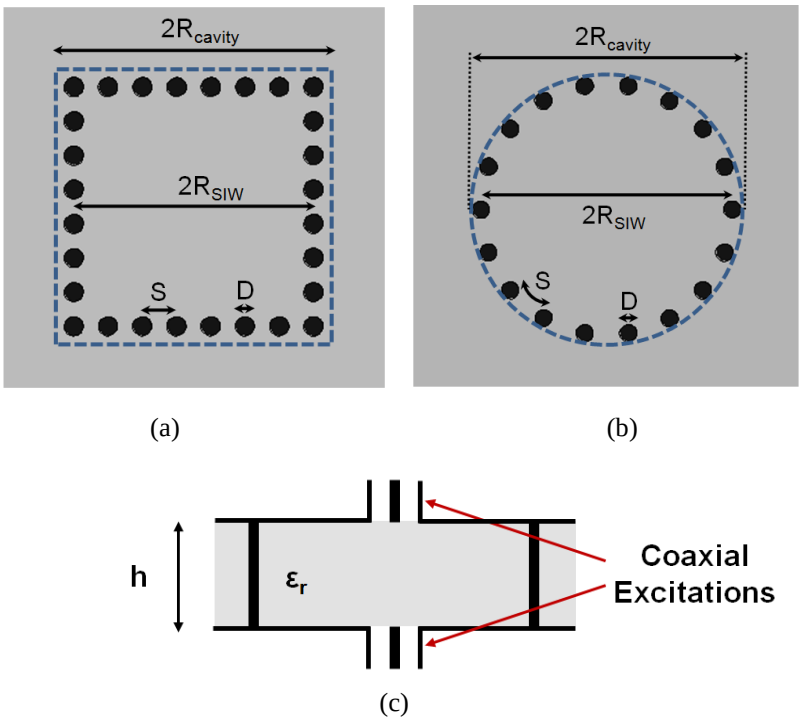
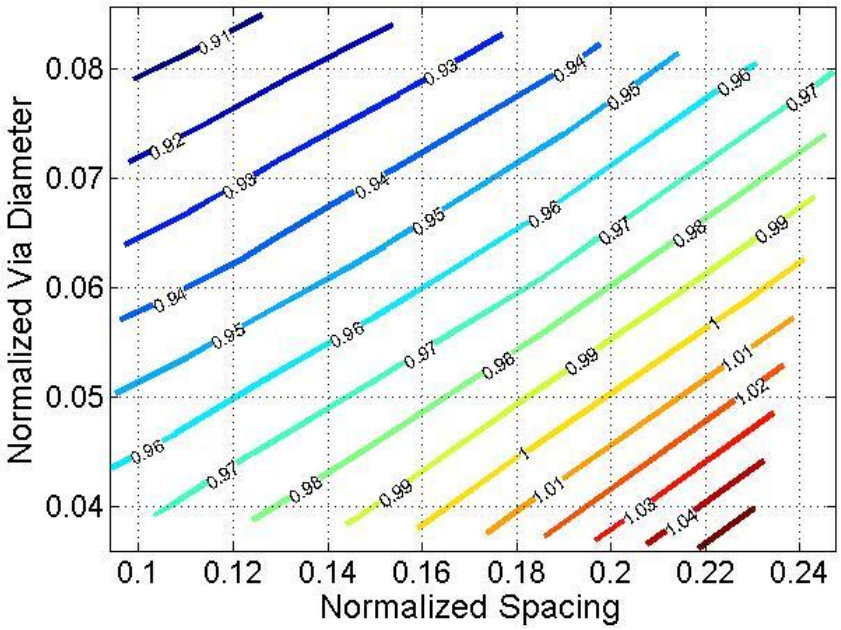
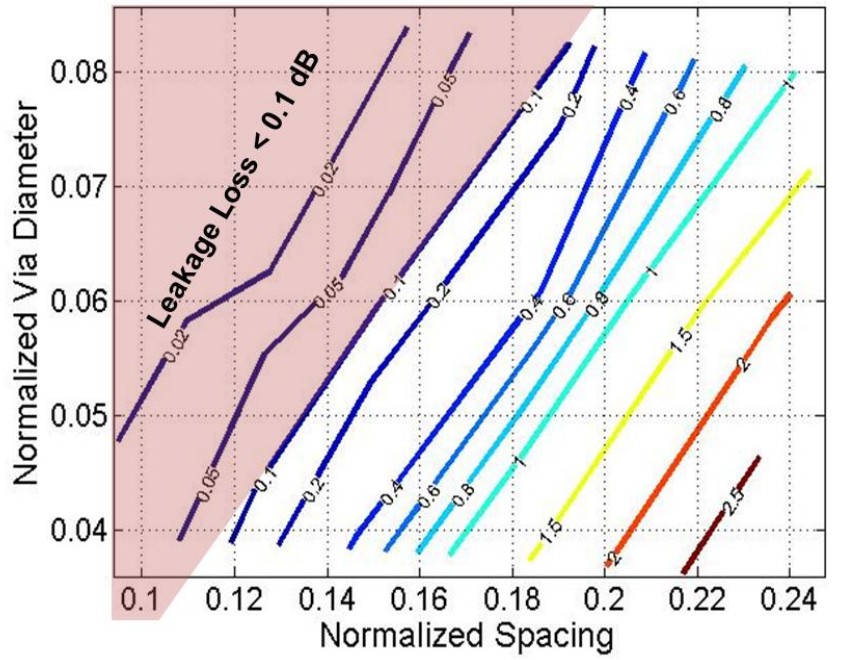


Figure 2.4 SIW cavities of (a) Rectangular, and (b) Circular shapes. (c) Cavity in a transmission setup with coaxial input and output excitations.

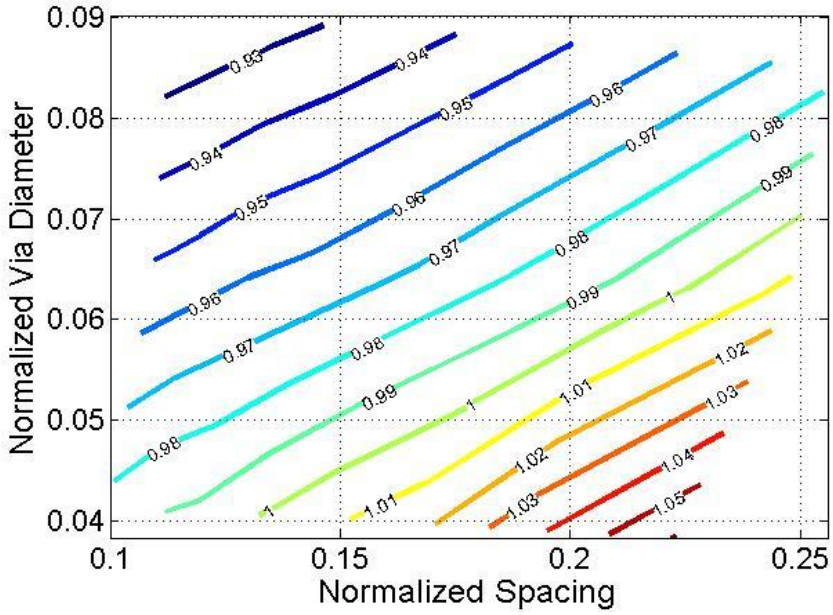


(a)

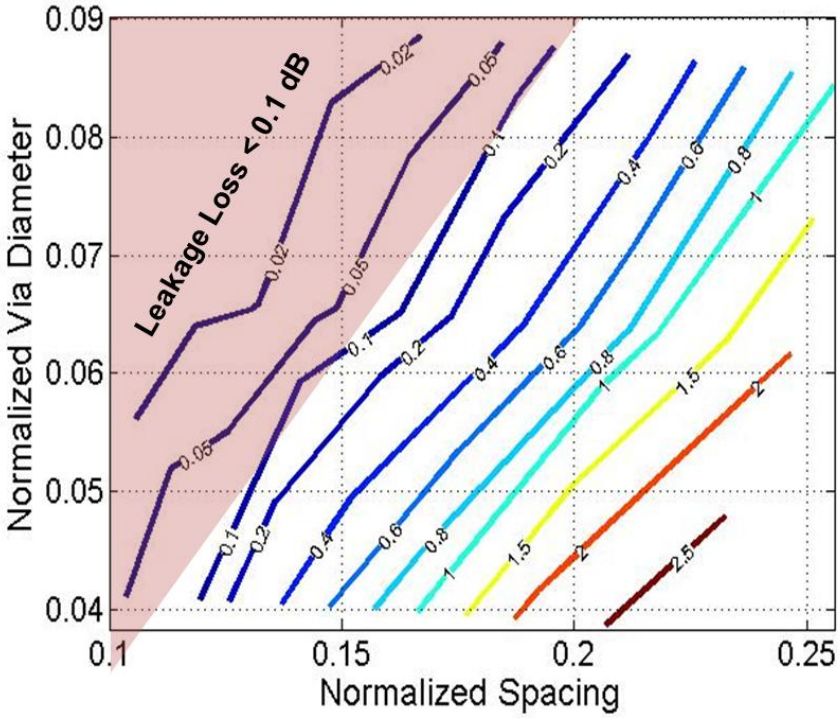


(b)

Figure 2.5 Characteristics of the rectangular SIW cavity in contour plots against the via holes diameter (D/λ_r) and spacing (S/λ_r) normalized to the resonance wavelength of the cavity, assuming ε_r =2.2 and h=1.57 mm. (a) Equivalence parameter to the solid wall cavity "P_{eq}". (b) Leakage loss in dB.



(a)



(b)

Figure 2.6 Characteristics of the circular SIW cavity in contour plots against the via holes diameter (D/λ_r) and spacing (S/λ_r) normalized to the resonance wavelength of the cavity, assuming ε_r =2.2 and h=1.57 mm. (a) Equivalence parameter to the solid wall cavity "P_{eq}". (b) Leakage loss in dB.

2.5 Design Approach

To that end, the design of the SIW cavity-backed patch antenna involves the selection of substrate properties (thickness; h and dielectric constant; ε_r) and determining the dimensions of the associated patch and cavity. The selection of the substrate properties is determined upon the required fractional bandwidth of the antenna. As far as the dielectric constant, the bandwidth is inversely proportional to $\sqrt{\varepsilon_r}$. Therefore, using a high dielectric constant substrate should be avoided, as it tends to trap the energy, thus increases the quality factor of the patch, which in return decreases the bandwidth and lowers the radiation efficiency of the antenna. This trapping effect has been previously reported in the case of conventional microstrip patches [3]. Meanwhile, the bandwidth, as expected, is proportional to the substrate thickness (cavity height) as a consequence of increasing the antenna's volume.

We have investigated here the four aforementioned topologies carrying out an extensive HFSS parametric study for each structure in the Ku-band frequency range. In our parametric study, the substrate thickness/cavity height was varied in discrete steps from $0.02\lambda_0$ to $0.1\lambda_0$ for several dielectric constant values namely; 2.2, 3.2 and 4.5. The cavity side length/diameter, and the excitation probe position x_p were adjusted in each step after changing the substrate thickness or dielectric constant to sustain a good match (i.e. S_{11}<-20dB). It was found that a choice of R=1.86a, R=2a, R=1.6a, and R=1.5a guarantees a good matching performance for the Rec-Rec, Rec-Cir, Cir-Cir, and Cir-Rec topologies, respectively.

Figure **2.7** shows the simulated fractional bandwidth and the associated resonant side length of the different structures versus the substrate thickness/cavity height (normalized to the resonant wavelength of the patch antenna) for different values of substrate dielectric constant. As expected, it is clear that increasing the substrate thickness would increase the fractional bandwidth while using relatively high dielectric constant substrates (ε_r=4.5) leads to a narrower fractional bandwidth compared to using a low dielectric constant substrate (ε_r=2.2). Meanwhile, using a high dielectric constant substrate tends to miniaturize the patch dimensions. In that perspective, the four different topologies exhibit similar trends, where a fractional bandwidth of better than 15% could be achieved by any of the different topologies upon using a low dielectric constant thick substrate of ε_r =2.2 and thickness $h=0.1\lambda_0$.

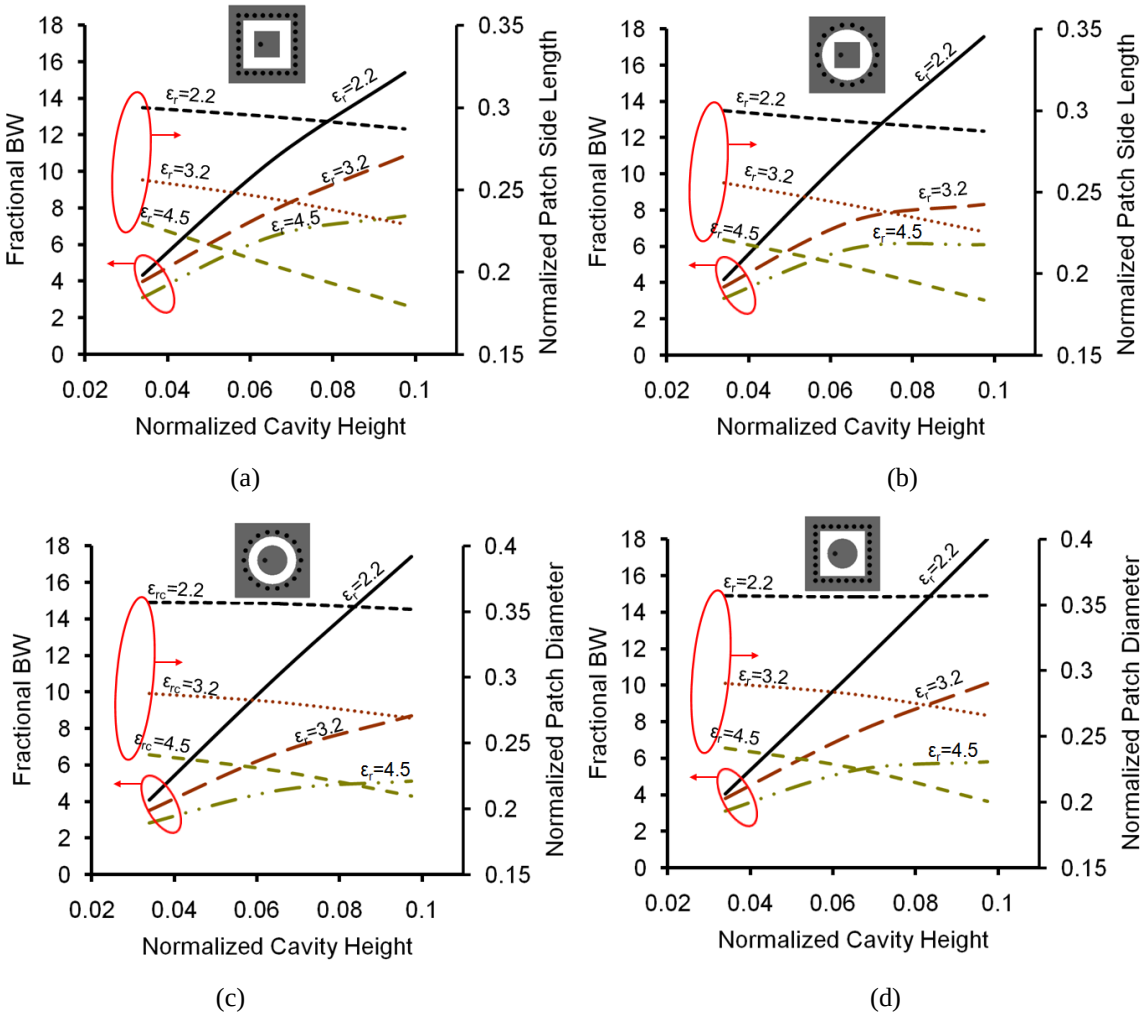


Figure 2.7 Design chart showing the fractional bandwidth and the normalized resonant patch side length $2a/\lambda_0$ vs. normalized cavity height h/λ_0 (a) Case of rectangular patch backed by rectangular cavity (assuming *R=1.86a*). (b) Case of rectangular patch backed by circular cavity case (assuming *R=2a*). (c) Case of circular patch backed by circular cavity case (assuming *R=1.6a*). (d) Case of circular patch backed by rectangular cavity (assuming *R=1.5a*).

2.6 Experimental Results

The proposed SIW cavity-backed patch antennas were designed to operate at the Ku-band range. Four different elements corresponding to the four different combinations of patch and cavity shapes were fabricated utilizing Rogers 5880 substrate of dielectric constant 2.2, loss tangent 0.0009 and thickness 1.575 mm. Standard SMAs of solder cup contact were employed to feed the elements. Table **2.2** shows the final design parameters of the different single elements. All the different single elements have a unit cell size of 19x19 mm^2. These different antenna structures were experimentally tested to examine their performance which will be reported in this section.

2.6.1 **Return Loss and Fractional Bandwidth Performance**

The return loss performance of the various fabricated single elements was evaluated by testing their reflection response using an Agilent E86386 network analyzer. Figure **2.8** shows the reflection coefficient response of the different single elements, where they exhibit fractional bandwidth of 9.2%, 9.2%, 10%, and 11% for the Rec-Rec, Rec-Cir, Cir-Cir and Cir-Rec single elements, respectively. As expected, using circular patches tend to give a wider bandwidth compared to the rectangular patches due to their larger patch areas (i.e. 55.4 mm^2 compared to 49 mm^2) and subsequently their volume under the antenna. It is also worth noting that the relatively widest achieved bandwidth is obtained when the circular patch is backed by a rectangular cavity structure (Cir-Rec).

2.6.2 **Normalized Gain Pattern**

Measurements of the antennas radiation patterns are shown in Figure **2.9** for the E-plane of the different single element topologies. The cross polarization levels are -27 dB, -27 dB, -24 dB, and -26 dB lower than the main polarization at broadside for the Rec-Rec, Rec-Cir, Cir-Cir and Cir-Rec single element, respectively. As expected, the rectangular patches relatively have better cross-pol performance compared to the circular ones.

Table 2.2 Design parameters of the different single elements (cavity height=1.575 mm)

	Rec-Rec	Rec-Cir	Cir-Cir	Cir-Rec
2a	7.00 mm	7.00 mm	8.40 mm	8.40 mm
2R	13.00 mm	14.00 mm	13.40 mm	12.60 mm
X_p	1.75 mm	1.75 mm	2.10 mm	2.10 mm
Patch Area	49 mm^2	49 mm^2	55.4 mm^2	55.4 mm^2

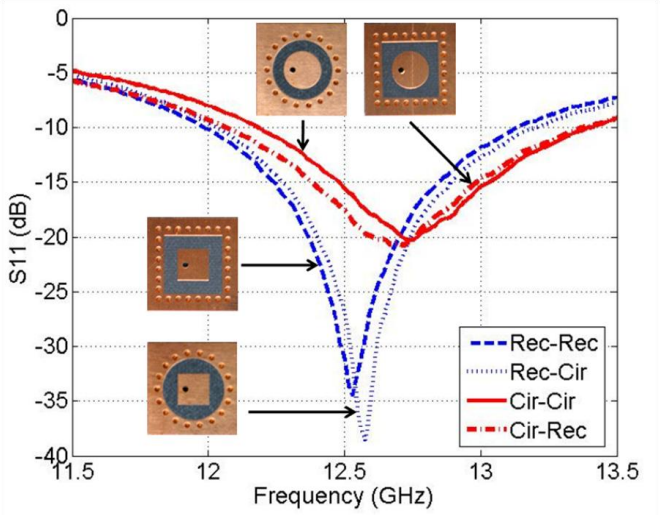


Figure 2.8 Measured reflection response of the different SIW cavity-backed patch antennas.

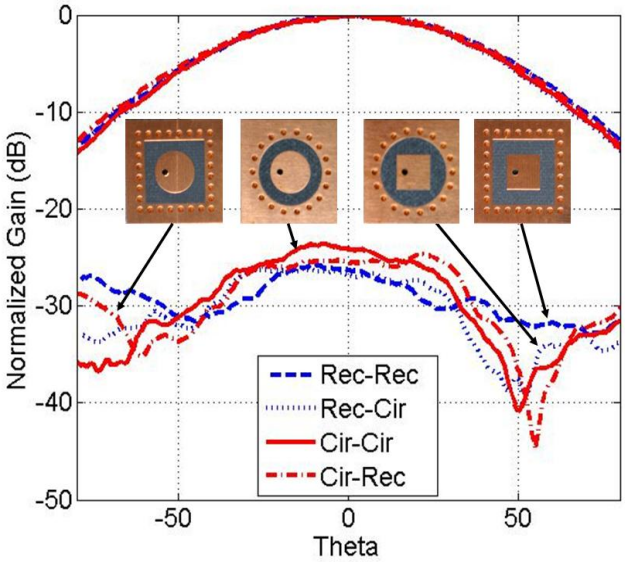


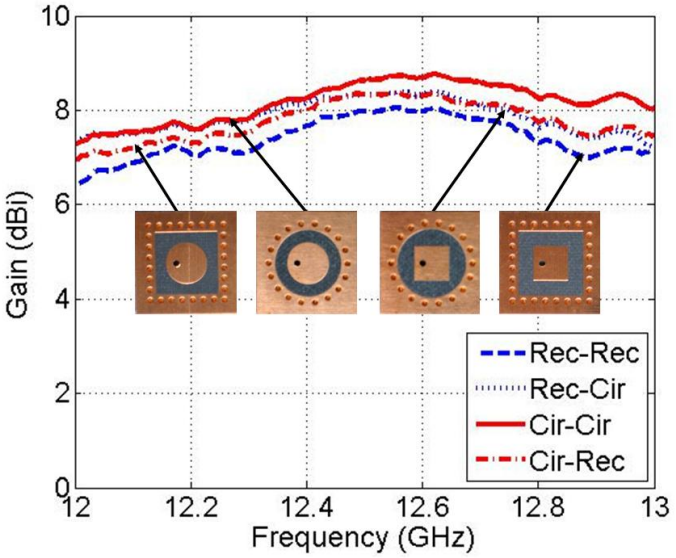
Figure 2.9 Normalized gain patterns of the different SIW cavity-backed patch antennas showing both the co-pol and x-pol performances.

2.6.3 **Gain versus Frequency and Aperture Efficiency**

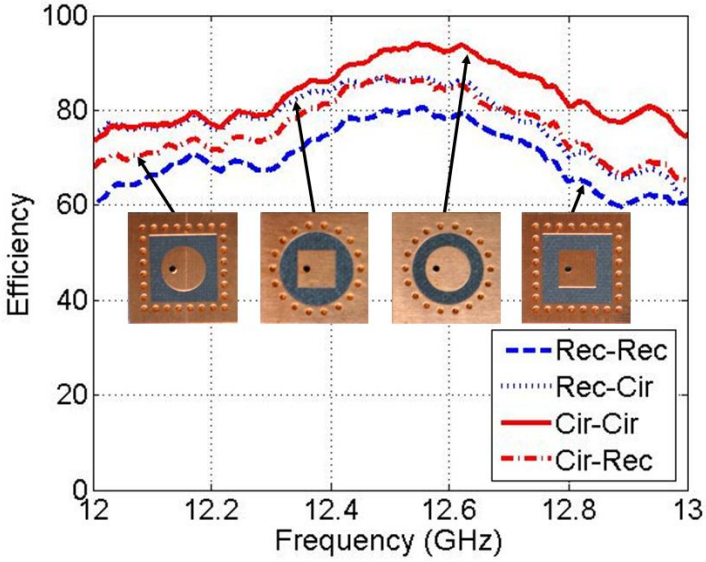
The measured gain and aperture radiation efficiency versus frequency are shown in Figure **2.10**. The different single elements exhibit gain of 8.0 dBi, 8.3 dBi, 8.3 dBi and 8.6 dBi at 12.5 GHz for the Rec-Rec, Rec-Cir, Cir-Rec, and Cir-Cir single elements, respectively, corresponding to aperture efficiency of 80%, 86%, 92% and 86%, respectively. It is observed that circular patches have better gain performance rather than the rectangular ones and patches gain could be enhanced if backed by circular cavities.

2.6.4 **Mutual Coupling**

Figure **2.11** shows the measured E-plane mutual coupling between two elements of the proposed cavity-backed patch spaced 19 mm apart, corresponding to about $0.8\lambda_0$, which is typically the array distance in most of fixed beam arrays. The mutual coupling between the two elements is below -27 dB along the Ku-band, which is significantly lower than its corresponding coupling in conventional patch arrays that is typically -20 dB, as indicated by Karmakar in [12] for the $0.8\lambda_0$ spacing, and is comparable to that attained by conventional metalized cavities [12]. Table **2.3** summarizes the performance of the different single elements. For designing arrays, feeding probes can be connected to a microstrip feed network that can be placed on the back of the structure, as we have demonstrated for instance for a 2x4 array in [64].



(a)



(b)

Figure 2.10 Measured (a) Gain and (b) Aperture efficiency vs. frequency of the different SIW cavity-backed patch antennas.

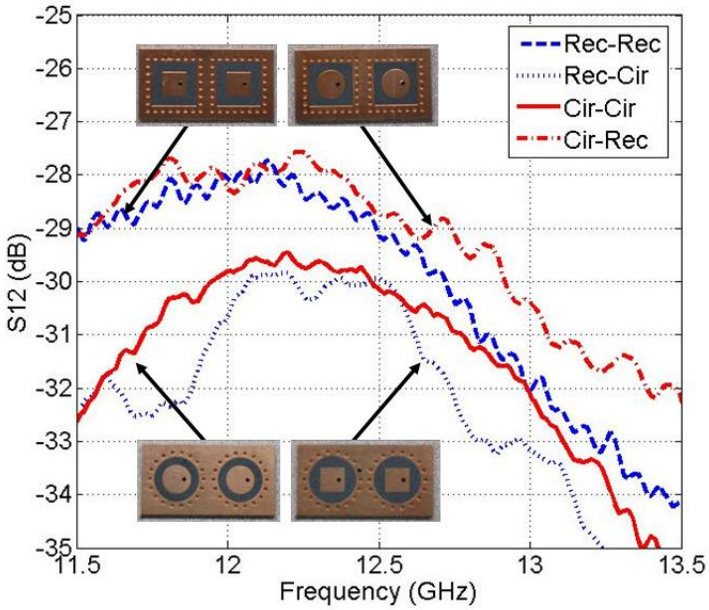


Figure 2.11 Measured E-plane mutual coupling coefficient of the different SIW cavity-backed patch antennas.

Table 2.3 Performance summary of the different probe-fed cavity-backed patch single elements

	Rec-Rec	Rec-Cir	Cir-Cir	Cir-Rec
FBW	9.2%	9.2%	10%	11%
Gain	8 dBi	8.33 dBi	8.62 dBi	8.33 dBi
Efficiency	80%	86%	92%	86%
X-POL	-28 dB	-28 dB	-24 dB	-26 dB
Mutual Coupling	-29 dB	-30 dB	-30.2 dB	-28.7 dB

2.7 Conclusion

A low-cost implementation of cavity-backed antennas has been proposed and experimentally verified using SIW technology. Four different single element designs, corresponding to the different combinations of patch and cavity shapes, have been fabricated and experimentally tested. The proposed cavity-backed patch antenna elements are comprised of only a single substrate where a patch is printed on the top substrate surface; while the cavity is implemented using plated via holes to emulate the conventional metalized cavities to back and surround the patches. The shapes of the patch and cavity have noticeable

effect on the bandwidth and x-pol performance of such elements. Developed design charts of the investigated four permutations of circular and rectangular structures have indicated that the substrate thickness (cavity height) could be selected to attain a given bandwidth for the patch up to 15% without degrading the patch efficiency, as the surface waves are suppressed by the SIW cavity.

The different fabricated prototypes have demonstrated fractional bandwidth larger than 9% and realized gain higher than 8 dBi corresponding to more than 80 % in aperture efficiency. Circular patches tend to have better bandwidth performance due to their larger volume contained under the patch; while the rectangular patches tend to give better cross-pol. On the other hand, the circular cavities tend to secure lower mutual coupling. Circular patch backed by circular cavity exhibits the highest gain of 8.6 dBi corresponding to 92% aperture efficiency. So, in our implementation of large arrays presented later we would use circular patches backed by circular cavities to obtain the highest possible gain.

Chapter 3 Microstrip-fed SIW Cavity-Backed Patch Arrays

In this chapter, the substrate-integrated waveguide (SIW) technology is utilized as an alternative low-cost approach to fabricate large cavity-backed patch arrays of microstrip feed. The proposed antenna arrays combine the attractive features of the conventional metalized cavity-backed patch arrays like surface wave suppression, high radiation efficiency, and enhanced bandwidth, yet with a low manufacturing cost. The design and performance of these arrays are compared to other conventional patch arrays of enhanced bandwidth. Performance limitations of the microstrip-fed structures are also explored.

3.1 Microstrip-Fed SIW Cavity-Backed Patch Antenna

Figure **3.1** shows a microstrip-fed version of the SIW cavity-backed patch antenna. The proposed microstrip-fed patch antenna elements, in contrast to the probe-fed elements previously demonstrated in Chapter 2, are comprised of a stack of two substrates, namely: a microstrip substrate and a cavity substrate. A trimmed square patch element was initially utilized in developing large arrays and will be presented in this chapter. Subsequently in the following chapters circular patches will be utilized.

The trimmed square patch is of side length *a,* and is printed on the microstrip substrate (of dielectric constant ε_{rs} and thickness h_s), as shown in Figure **3.1**. The ground plane of the microstrip substrate and the top layer of the cavity substrate have a common circular opening of radius *R* underneath the patch. Many via holes spaced along the circular opening are laser-drilled in the cavity substrate (of dielectric constant ε_{rc} and thickness h_c), and are platted-through constituting the SIW circular cavity backing the patch, as shown in Figure **3.1**.

To that end, the design of the SIW cavity-backed patch antenna involves the selection of the properties of both substrates (i.e. its thickness and dielectric constant) and the dimensions of the patch and cavity. In that perspective, the use of a low-loss low dielectric constant thin substrate ~ 0.02 λ_0 is preferred to minimize both dielectric and surface wave losses. In our demonstration here, we have used a 0.381 mm-thick substrate (corresponding to 0.016 λ_0), and of dielectric constant equals 2.2 for the microstrip substrate.

Similar to the probe-fed antennas demonstrated in Chapter 2, the bandwidth of the antenna is mostly dependent on the cavity substrate thickness and dielectric constant given that thin microstrip substrate is used. As far as the dielectric constant, the bandwidth is inversely proportional to $\sqrt{\varepsilon_r}$, which is very

similar to the conventional microstrip patches [4]. Therefore, on one hand it is recommended to use a low dielectric constant substrate for the SIW cavity to achieve an adequate bandwidth to cover the DBS band. On the other hand, a dielectric filled cavity will have a miniaturizing effect on the patch size.

Similar to the design rule developed in Chapter 2, for designing a Rec-Rec cavity-backed patch element, we will use: $R=0.84a$ where R is the cavity radius and a is the patch side length. This is slightly different from the rule used before in Chapter 2 for the Rec-Rec cavity-backed patch because here the patch is trimmed. Subsequently, we have carried out a parametric study for the effect of the cavity height on both the bandwidth and patch resonant side length, as shown in Figure **3.2**. As expected, the effective bandwidth of the cavity-backed patch antenna structure is a function of the cavity height, as increasing the cavity height can lead to a wider bandwidth due to the volume increase of the antenna. Figure **3.2** clearly shows that the antennas' fractional bandwidth is less than 2%, when the cavity height is zero, and it increases significantly to about 9% upon utilizing a cavity height of $0.12\lambda_0$ in height.

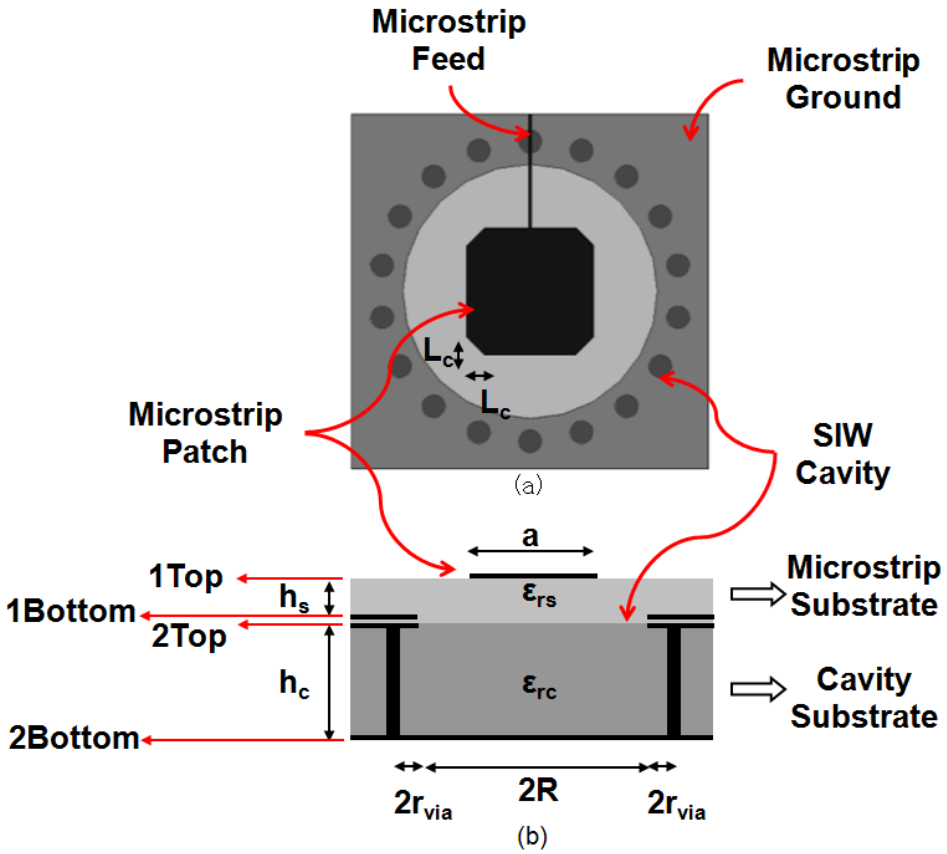


Figure 3.1 Microstrip-fed SIW cavity-backed patch single element. (a) Top view. (b) Side view.

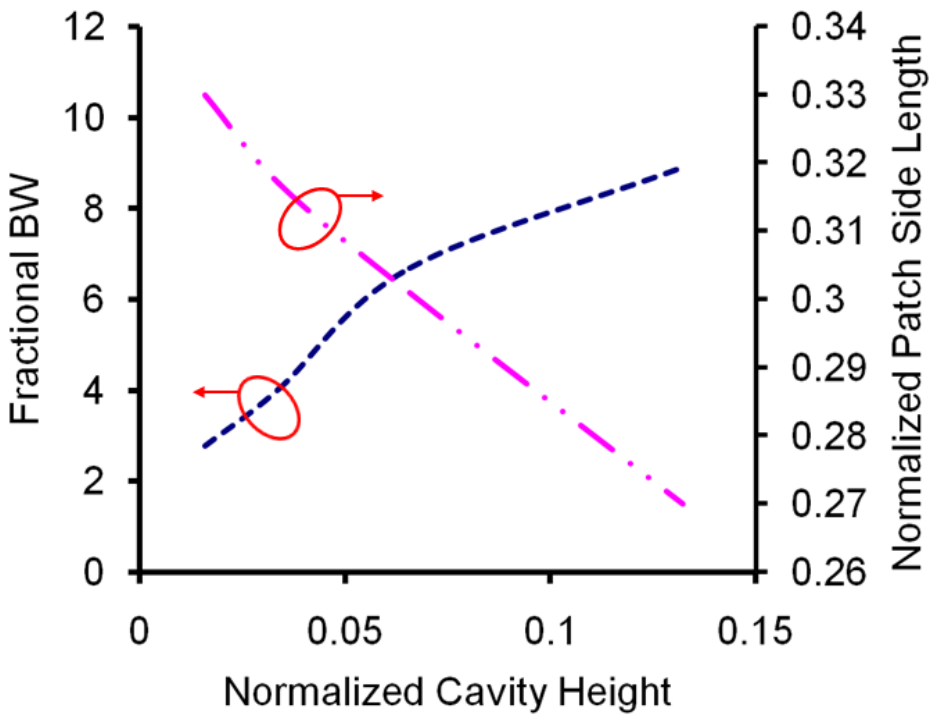
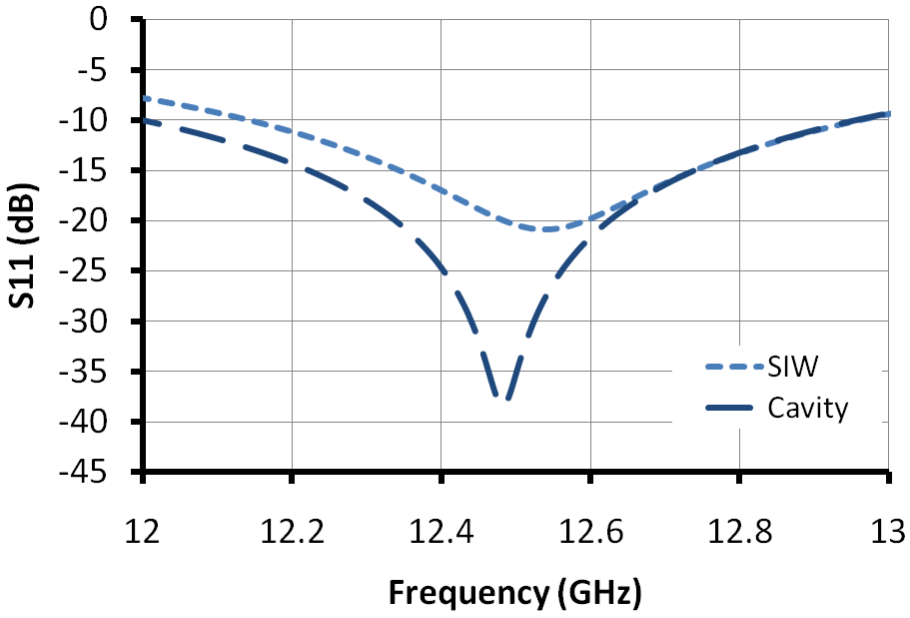


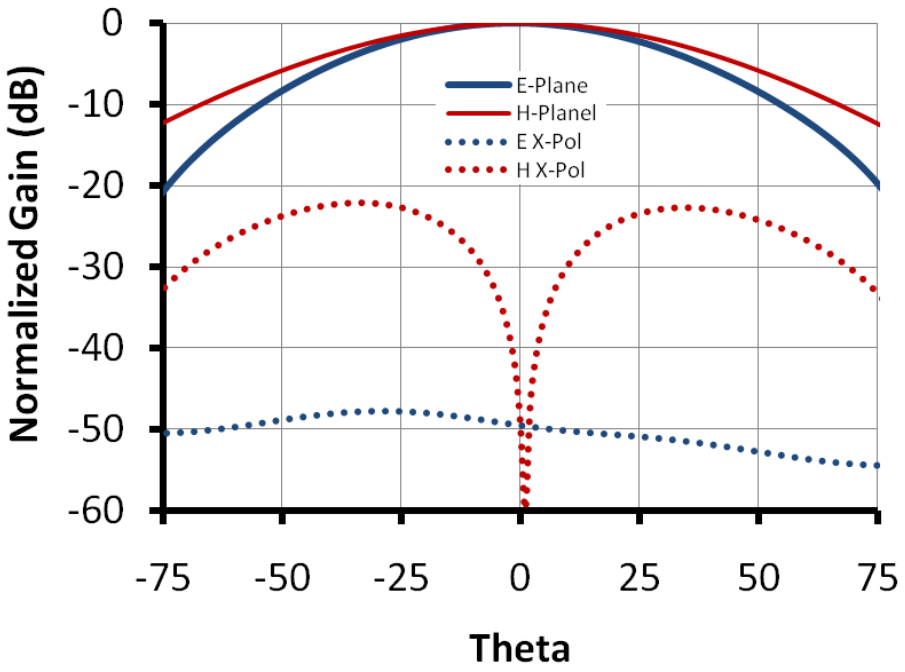
Figure 3.2 Design chart showing the fractional bandwidth vs. normalized cavity height of the SIW cavity-backed patch and the normalized resonant side length of the patch for the single element.

In our single-element design to achieve about 7% fractional bandwidth, it was adequate to use a cavity height of $0.066\lambda_o$ (i.e. h_c=1.575 mm), a patch side length of 7.2 mm, and using via holes of r_{via}=0.635 mm. The associated single element gain is 8.0 dBi (assuming h_s= 0.381 mm, ε_{rs}=2.2, and ε_{rc}=2.2); which is equivalent to an 80% aperture efficiency.

The effect of using the emulated cavity was numerically evaluated and compared to the relevant case of air-filled cavity with the following dimensions; patch side length a= 9 mm, and R=7.2 mm assuming same microstrip substrate properties (h_s= 0.381 mm, and ε_{rs}=2.2) and with the same cavity height (i.e. h_c=1.575 mm), however the cavity is air-filled (i.e, ε_{rc}=1). The reflection coefficients of both the substrate-integrated and metalized cavity structures were calculated using HFSS simulation tool and are shown in Figure **3.3**(a). Obviously, the bandwidth of the air filled metalized cavity structure is slightly larger than that of the SIW one, which is due to the dielectric substrate loading as it tends to trap the energy more than the air, and subsequently increases the quality factor of the patch and thus decreases the antenna's bandwidth and lowers its radiation efficiency [3]. Figure **3.3**(b) also shows the gain patterns of the SIW cavity-backed patch element, which demonstrates very low cross-polarization level. It is worth noting also that the SIW cavity-backed structure has slightly lower gain (8.0 dBi) compared to the solid wall cavity-backed patch (8.3 dBi) again due to the dielectric loading.



(a)



(b)

Figure 3.3 Microstrip-fed single element SIW cavity-backed patch. (a) Reflection response. (b) Gain pattern..

3.2 Array Configuration

The previously discussed microstrip-fed single element antenna was utilized to design large arrays. Figure **3.4** illustrates the proposed SIW cavity-backed array for an 8x8 array with its constituting layers spaced apart. Similar to the single element antenna, a stack of two substrates: a "microstrip substrate" and a "cavity substrate" is utilized and the bottom layer of the microstrip substrate and the top layer of the cavity substrate have common circular openings underneath the patches. In the developed design procedure, we have used a 2x2 sub-array rather than a single element as a module for designing larger arrays. For example, the 64 elements of the array are subdivided into sixteen 2x2 sub-arrays, as shown in Figure 3.4. A probe feed is employed to launch the microwave signal to the center of a microstrip feed network which is then utilized to distribute the microwave energy to the patch elements.

3.2.1 **Microstrip Feed Network**

A simple microstrip binary feed network with quarter wave transformers is utilized to direct the signal from the central feed to the patches. The central feed is an integrated 50Ω coaxial probe feed topology, similar to that proposed in [65], where many via holes were implemented to emulate the outer wall/shield of the coaxial feed probe. The structure provides a smooth transition and minimal unwanted feed radiation loss. For illustration, a 3-D model of the one-to-four microstrip divider network employed in the 2x2 sub-array is shown in Figure **3.5**(a).

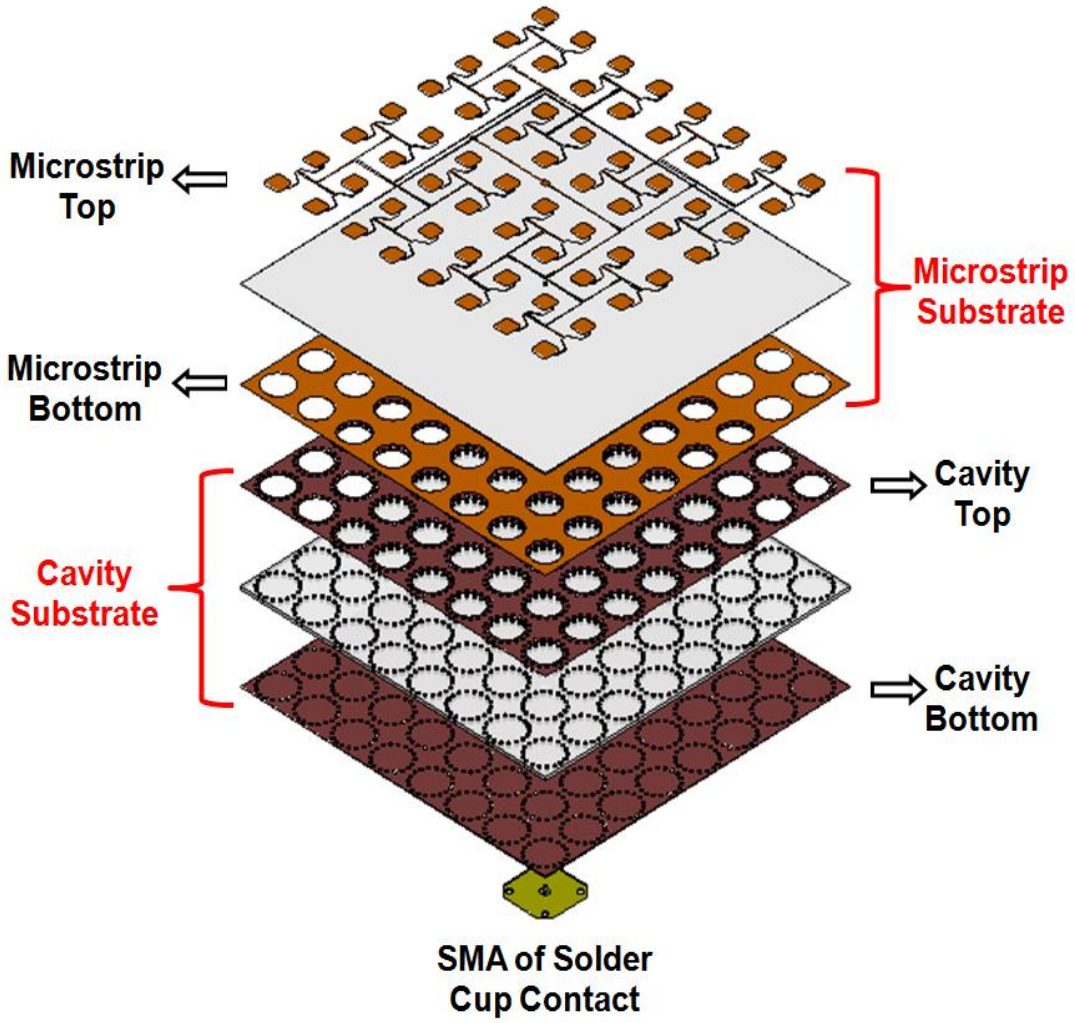
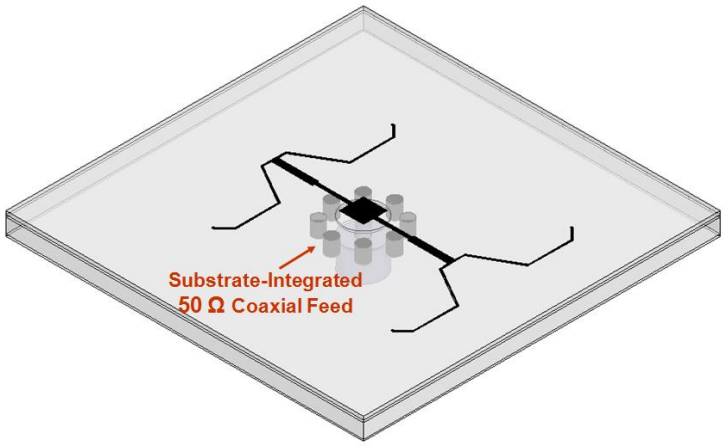
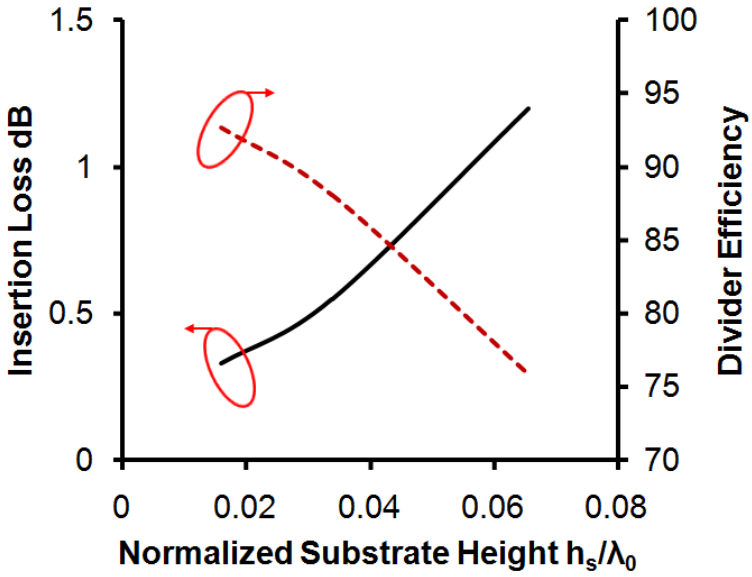


Figure 3.4 3D model of the SIW cavity-backed patch 8x8 array showing the constituting layers spaced apart.



(a)



(b)

Figure 3.5 Basic one-to-four probe-fed microstrip feed network. (a) 3D model. (b) Simulated loss and efficiency performance vs. the normalized substrate thickness (simulated at Ku-band for ε_{rs}=2.2, and tanδ=0.0009).

3.3 Array Design Approach

A modular design approach was adopted in attaining the arrays, where a 2x2 sub-array module is repeatedly cascaded along the x and y directions to constitute larger arrays. Very similar to the single element design, the design of the SIW cavity-backed patch sub-array involves the selection of both substrates—their thicknesses and dielectric constants, and the determination of the patch and cavity dimensions. In this section, we will elaborate on the 2x2 sub-array design guidelines.

3.3.1 **Microstrip Substrate Properties**

The microstrip substrate properties (thickness h_s and ε_{rs}) determine the loss performance of the feed network. For instance, the insertion loss of the one-to-four divider, shown in Figure **3.5**(a), was calculated at Ku-band as a function of the substrate thickness, as shown in Figure **3.5**(b). In this calculation, the line impedances of the divider *w* constantly adjusted based on the utilized substrate thickness to keep a good input match. It is clear from Figure **3.5**(b) that increasing the microstrip substrate thickness beyond $0.02\lambda_0$ would lead to an increased insertion loss for the divider due to surface wave propagation. Even though the conductor loss would decrease with increasing the substrate thickness, but the additional larger losses of the surface waves would become more pronounced and would cause significant efficiency degradation of the divider performance. As an example, using a thin substrate of $0.016\lambda_0$ would imply a 0.3dB insertion loss for the divider. But, this feed insertion loss would increase to 1dB if a four times thicker substrate is employed. Therefore, it is imperative to use a relatively thin low-loss dielectric constant microstrip substrate to minimize the surface wave losses of the feed network; which consequently would lead to maximizing the antenna's radiation efficiency.

3.3.2 **Cavity Substrate Selection**

Similar to the single element design, the selection of the cavity substrate -- thickness h_c and dielectric constant ε_{rc} is determined by the required fractional bandwidth of the antenna. The bandwidth is inversely proportional to the square root of the dielectric constant. Subsequently, using high dielectric constant substrates should also be avoided here, as well, as they tend to trap the energy which increases the quality factor of the patch, decreases the bandwidth, and lowers the antenna radiation efficiency. This effect has been reported before for conventional microstrip patches [3].

Figure **3.6** shows the simulated fractional bandwidth (-10 dB bandwidth of S_{11} normalized to its center frequency) of the basic 2x2 sub-array versus the cavity substrate thickness assuming ε_{rs}= 2.2, h_s=$0.016\lambda_0$, for a family of ε_{rc} of 2.2, 3.2 and 4.5. It is clear from Figure **3.6** that by increasing the cavity substrate thickness, the fractional bandwidth of the antenna can be enhanced. For instance, upon using a low dielectric constant substrate (ε_{rc} =2.2) with height h_c=$0.1\lambda_0$, the fractional bandwidth has increased to

approximately 13% compared to only 2% for the conventional microstrip antenna without backing cavities (i.e. h_c=0). For even further bandwidth enhancement, stacking patches at different layers could be used [10, 66], where over 18% fractional bandwidth has been achieved in [66]. Even though stacking more layers is compatible with SIW, it can render a very thick overall antenna profile.

3.3.3 **Cavity and Patch Dimensions Selection**

The previous parametric study for a single element design discussed in Chapter 2, was extended to select optimum cavity and patch dimensions for the sub-array, where the 2x2 basic sub-array was numerically simulated assuming ε_{rs}= 2.2, h_s=0.38 mm ($0.016\lambda_0$), ε_{rc}= 2.2, and h_c=1.58 mm ($0.066\lambda_0$). In this parametric study, the patch side length was fixed at 7.5 mm, while the cavity radius was varied from 5.7 mm to 6.3 mm in 0.3 mm steps. The corresponding reflection coefficient performance is shown in Figure **3.7**, and indicates an adequate matched performance for a cavity radius corresponding to *R=0.84a* (where *R* is the cavity radius, and *a* is the patch side length). Hence, we adopted this ratio and developed a full design chart for the side length selection, as shown in Figure **3.6**.

The developed design chart could be used as follows:-

- Select the cavity substrate thickness based on the required bandwidth.
- Accordingly, select the patch resonant side length *a*.
- Subsequently, the other design parameters can be calculated from $R = 0.84 \cdot a$, and $L_c = a/5$.

Meanwhile, for attaining larger arrays, the designed 2x2 sub-array module can be simply replicated along the x and/or y dimensions, however fine optimization might be required for larger arrays.

Subsequently, 2x4, 4x4, and 8x8 SIW arrays were designed to operate at the Ku-band with a fractional bandwidth better than 9%. The final design parameters are: microstrip substrate has h_s=0.38 mm and ε_{rs}= 2.2, cavity substrate has h_c=1.58 mm and ε_{rc}= 2.2, patch side length a=7.5 mm, and L_c =1.5 mm, array spacing d=19 mm, and cavity radius R=6.3 mm.

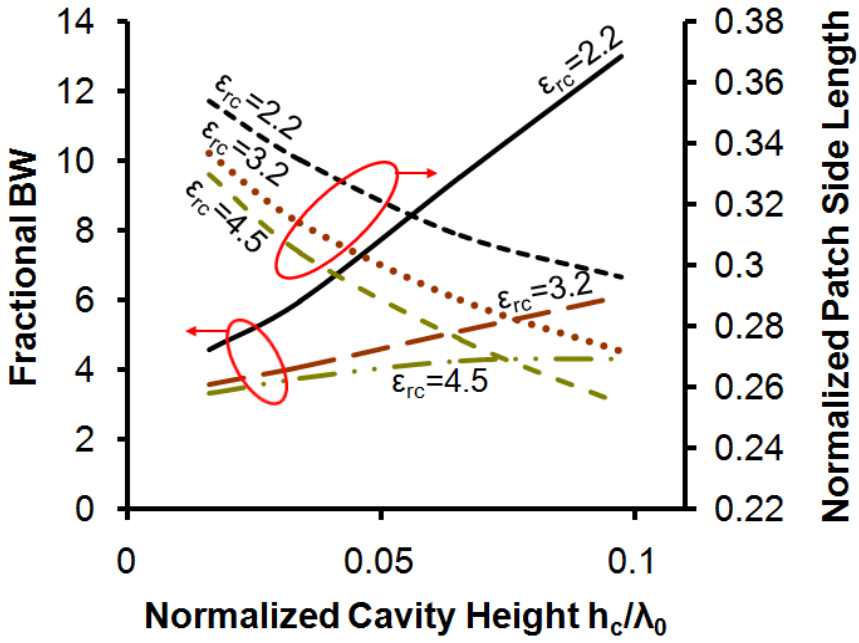


Figure 3.6 Design chart showing the fractional bandwidth and the normalized patch side length a/ λ_0 vs. normalized cavity height adopting the "R=0.84a" design rule (assuming h_s= 0.016λ_0, ε_{rs}=2.2, d~0.8λ_0, L_c=a/5).

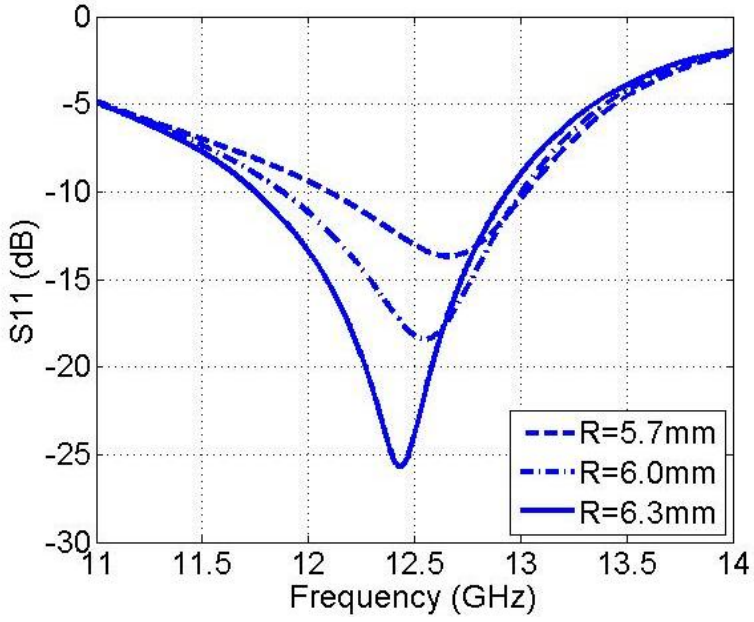


Figure 3.7 Simulated reflection coefficient of the 2x2 array with different cavity sizes varied from 5.7 mm to 6.3 mm with a step of 0.3 mm (assuming h_s= 0.016λ_0, ε_{rs}=2.2, d~0.8λ_0, L_c=a/5, h_c=0.066λ_0, ε_{rc}=2.2).

3.4 Viability of the Proposed SIW Antenna

A thorough investigation using HFSS [67] has been carried out to provide performance comparison of the proposed SIW cavity-backed structures relative to other structures commonly used to enhance the patch's inherent limited bandwidth.

3.4.1 **Single-Element Comparison**

Figure **3.8** shows the general case of a suspended substrate patch backed by a metalized cavity. Obviously, this general case reduces to the special case of a microstrip structure, upon setting h_a=0 and h_c=0, or to the suspended structure, upon setting h_c=0, or finally to the metalized cavity-backed structure upon setting h_a=0. In our comparison, we kept the total height $h=h_s+h_a+h_c$ and the aperture size the same for the different investigated structures and equals to that of the SIW single element (h=1.96 mm, aperture area=19x19 mm^2). This comparison criterion is based on the fact that the antenna bandwidth is generally proportional to the volume of the microstrip antenna [2]. The simulated performance at 12.5 GHz of these various structures is shown in Table **3.1** indicating their fractional bandwidth, realized gain, and achieved aperture efficiency.

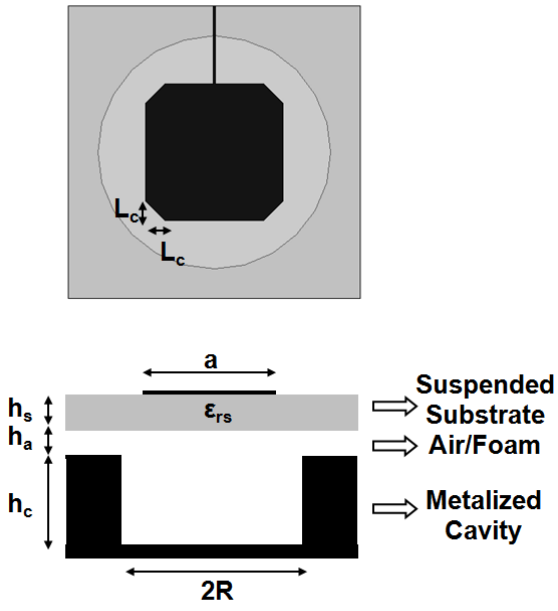


Figure 3.8 Metalized cavity-backed suspended patch single element

Table 3.1 Performance comparison of the different microstrip-fed single elements at 12.5 GHz

	FBW	Gain	Aperture Efficiency
Microstrip Patch ε_{rs}=2.2, h_s=1.96 mm, h_a=0, h_c=0	6.2 %	6.3 dBi	54 %
Suspended Patch ε_{rs}=2.2, h_s=0.38 mm, h_a=1.58 mm, h_c=0	7.7 %	7.6 dBi	73 %
Metalized Cavity-Backed Patch ε_{rs}=2.2, h_s=0.38 mm, h_a=0, ε_{rc}=1, h_c=1.58 mm	6.9 %	8.3 dBi	86 %
Cavity-Backed Suspended Patch ε_{rs}=2.2, h_s=0.38 mm, h_a=0.79 mm, ε_{rc}=1, h_c=0.79 mm	8.5 %	7.7 dBi	75 %
SIW Cavity-Backed Patch ε_{rs}=2.2 , h_s=0.38 mm, ε_{rc}=2.2, h_c=1.58 mm	6.6 %	8.0 dBi	80 %

We can infer the following from Table **3.1**:

- As expected, the conventional microstrip patch built on a thick substrate has a degraded gain performance due to significant surface wave losses.
- Upon using the suspended patch topology a noticeable increase in bandwidth, gain, and efficiency is achieved.
- The highest gain (8.3 dBi) and aperture efficiency (86%) are achieved upon using the metalized-cavity, but with a slight decrease in the associated fractional bandwidth compared to the suspended case.
- The largest fractional bandwidth of 8.5% is attained using the hybrid cavity-backed suspended patch, however with a realized gain of 7.7 dBi -- lower than the metalized cavity-backed patch case.
- Finally, the proposed SIW cavity-backed patch exhibits a gain of 8.0 dB, corresponding to an aperture efficiency of 80%, slightly short of that of the metalized cavity-backed case but better than the other suspended or microstrip cases. The fractional bandwidth is 6.6% which is also, as expected, slightly lower than the metalized cavity-backed and suspended cases.

In the aforementioned simulations, we have included the dielectric loss for the different single element cases, as we assumed a loss tangent of tan δ = 0.0009, which amounts to less than 0.1 dB, i.e. insignificant loss contribution.

Clearly, the proposed SIW single element is far superior to the conventional microstrip patch structure as the implemented SIW cavity efficiently suppresses the surface waves, similar to the effect of

band-gap structures [68-70]. Meanwhile, the SIW structure is simple to fabricate compared to the metalized cavity-backed case and is also easy to assemble compared to the suspended structures cases.

3.4.2 **Feed Network**

We have also compared the losses of the feed lines for the five topologies under investigation. The feed network would be either based on microstrip lines, for the cases of: the conventional microstrip, the metalized cavity-backed, and the SIW cavity-backed patch antennas; or suspended lines for the cases of: the suspended and the cavity-backed suspended patches. Hence as a first step to develop general design rules, we have evaluated the insertion loss of both the microstrip and suspended lines as a function of their heights above the ground plane.

Generally, it is preferable to use relatively narrow feed lines in order to decrease the mutual coupling between the microstrip feed network and the radiating elements, however increasing the height of these substrates would typically lead to unacceptable wide lines if the impedance levels of the feed network lines are the same at all heights. Alternatively, in our comparative study, we kept the lines' widths constant and presented the corresponding lines' impedances for a strip width of w= 0.33 mm, as indicated in Figure **3.9**, for both the microstrip and suspended structures cases. As expected, the suspended lines have better performance, when compared to the microstrip lines due to their lower losses [16]. However, both the microstrip and suspended lines have significant losses upon using thicker substrates (i.e. > $0.03\lambda_o$), as shown in Figure **3.9**(c), due to the associated surface waves' high loss.

From that point of view, the cavity-backed patch structures proved to be advantageous over the thick substrate or suspended substrate topologies as the feed microstrip substrate can be kept relatively thin, while the cavity height could be adequately changed independently to achieve the required bandwidth design goal.

We also conclude that the feed losses of the thick microstrip case (h_f=1.96 mm) are significantly worse than the other structures followed by the suspended case (h_f=1.96 mm), and then the cavity-backed suspended patch case, as it has a smaller height above the ground (h_f=1.05 mm), then finally the SIW and metalized cavity-backed structures (h_f=0.38 mm).

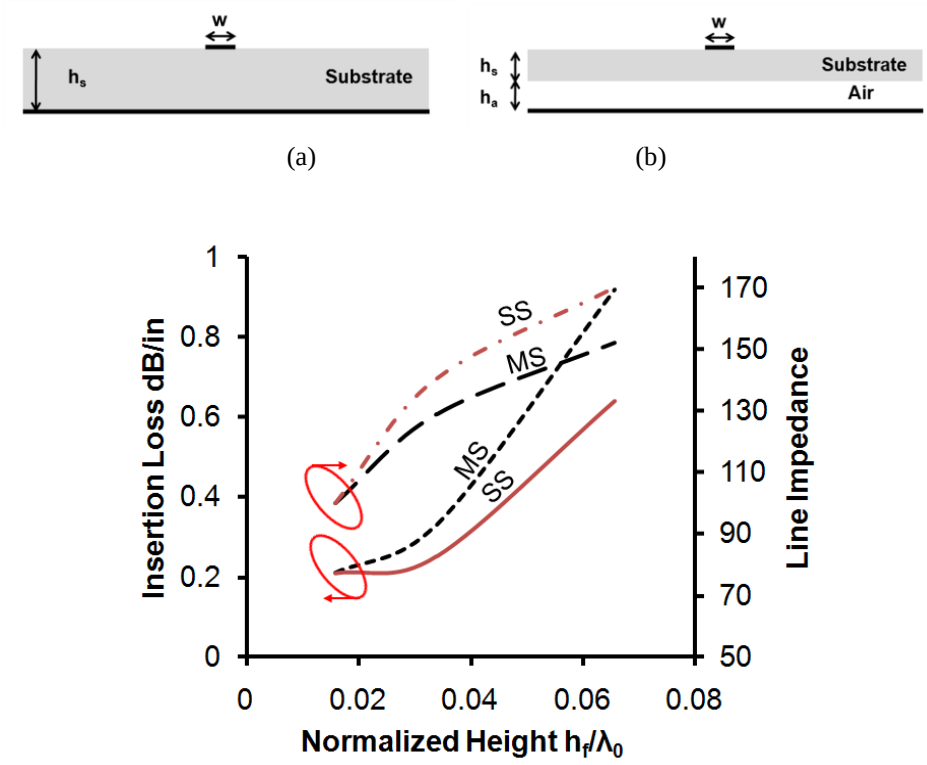


Figure 3.9 Feed loss comparison between microstrip and suspended lines. (a) Microstrip line. (b) Suspended line. (c) Simulated insertion loss and impedance level vs. the normalized height h_f/λ_0 ($h_f=h_s$ for the microstrip line case and $h_f=h_s+h_a$ for the suspended line case with h_s=0.38 mm).

3.4.3 **2x2 Sub-array**

Figure **3.10** depicts a comparison of the fractional bandwidth and normalized resonant patch side length between the 2x2 SIW sub-array (assuming ε_{rs}=2.2) and the corresponding air-filled metalized cavity-backed, and the suspended cavity-backed cases. Again, the SIW sub-array has a relatively narrow fractional bandwidth compared to the other two cases, while the suspended cavity-backed patches case has the widest bandwidth, which is expected from the single-element performance previously demonstrated in section 3.4.1. Additionally, the SIW structure has a smaller patch size because of the miniaturization effect of the dielectric substrate loading of the backing cavity [71].

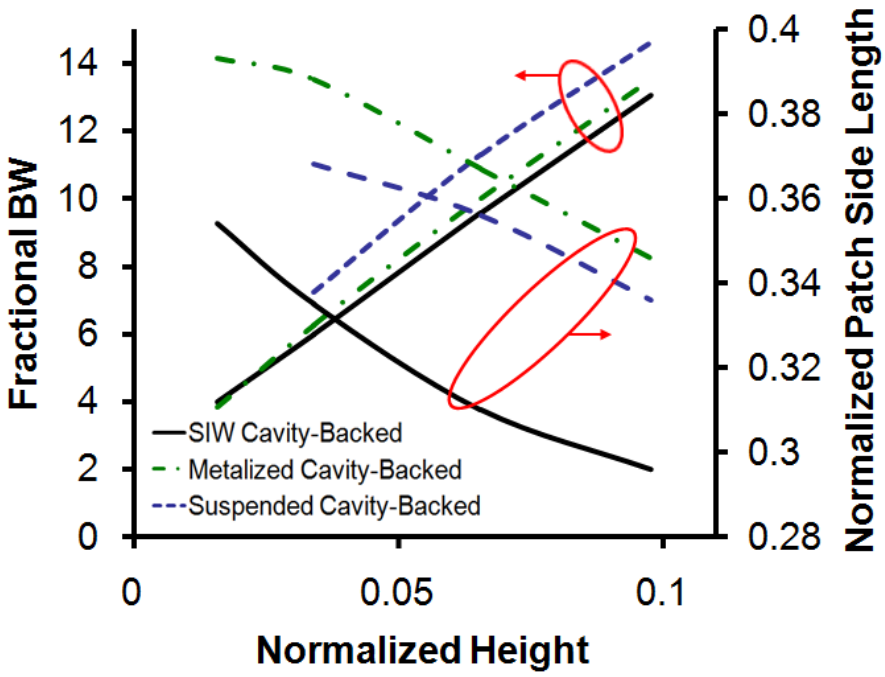


Figure 3.10 Comparison between the SIW cavity-backed, metalized cavity-backed, and suspended cavity-backed 2x2 sub-arrays (assuming h_s= $0.016\lambda_0$, ε_{rs}=2.2, d~$0.8\lambda_0$, L_c=a/5) as far as the fractional bandwidth and the normalized resonant side length vs. normalized cavity height (for the suspended cavity case, the height is the cavity height plus the air layer thickness).

3.4.4 **Larger Arrays**

Larger arrays of 4x4 and 8x8 sizes were numerically simulated taking into account their associated feed network losses. Table **3.2** compares the realized gain of the different five topologies for the different sized Ku-band arrays. Their corresponding aperture efficiency is plotted versus the array size in Figure **3.11**.

Obviously, the SIW cavity-backed antennas have comparable performance to the cavity-backed suspended substrate arrays, while the cavity-backed patches with metallic cavities have the best overall performance, as shown in Figure **3.11**, delivering the highest aperture efficiency. SIW cavity-backed arrays come next with an approximately 8% reduction in efficiency for the same antenna height/thickness of 1.96 mm. Suspended cavity-backed arrays is slightly lower than the SIW arrays in efficiency -- with approximately 2% reduction. Clearly, the suspended arrays and the thick microstrip arrays are far inferior to the other structures with the aperture efficiency degradation becomes worse for large arrays (i.e. larger than 8 elements) as the lines of the feed network get longer and accumulate more losses.

Table 3.2 Simulated realized gain (dBi) of the different arrays at 12.5 GHz

N	Microstrip Array	Suspended Array	Cavity-Backed Suspended Array	SIW Cavity-Backed Array	Metalized Cavity-Backed Array
2x2	12.5	13.8	14.0	14.0	14.3
4x4	17.4	18.7	19.1	19.5	19.9
8x8	20.3	23.2	24.5	24.7	25.5

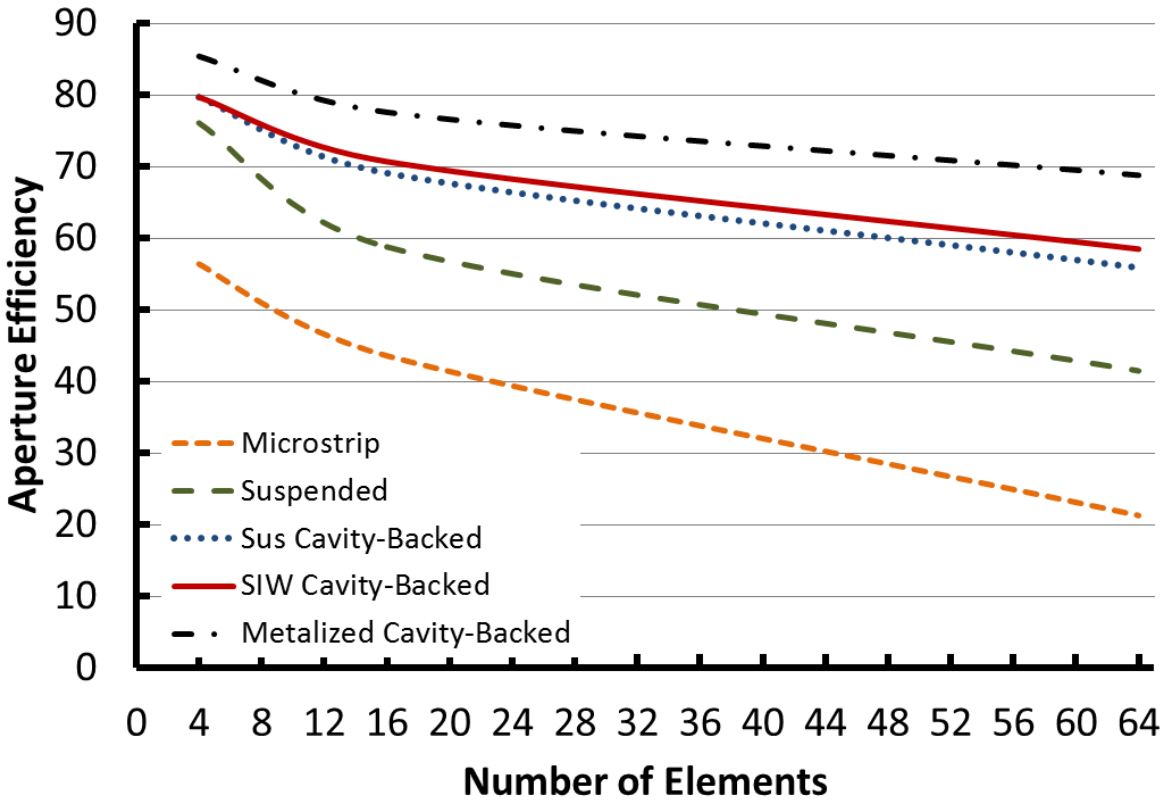


Figure 3.11 Calculated aperture efficiency versus frequency of the different array structures

Based on the above analysis, we could approximately extrapolate a rough empirical formula to estimate a theoretical aperture efficiency of large arrays of SIW cavity-backed patches (i.e. larger than 16 elements) as:-

$$\text{Efficiency}_{SIW}(\%) = -0.183N + 80.5 \quad (3\text{-}1)$$

Where N is the number of elements in the array

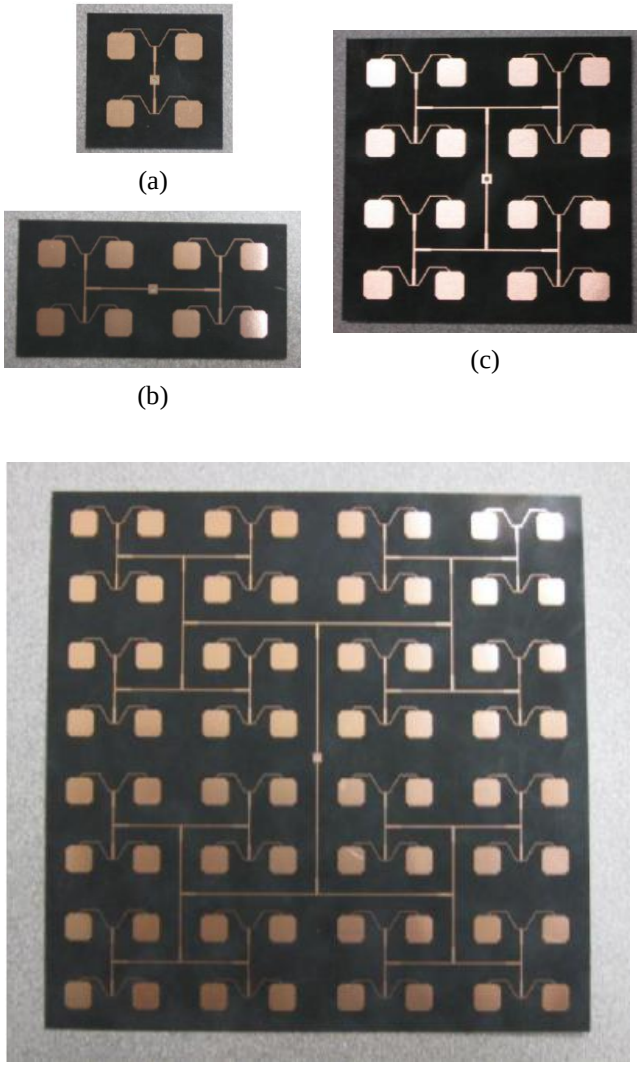
Upon that we could roughly estimate the theoretical aperture efficiency for even larger arrays (i.e. larger than 64 elements). For instance, the aperture efficiency of 64 elements array would be approximately 58%, while it would drop sharply to 34% for 256 elements array, which is not acceptable. Therefore, we could conclude that going to large arrays >64 elements would need better feed topology to have lower feed loss; thus achieving better aperture efficiency, which will be pursued in the next Chapter. It worth noting also, that the effect of the assemblage loss and any misalignment losses are not accounted for here and could lead to pronounced effects especially for large arrays.

3.5 Experimental Results

Based on the previously designed 2x2 sub-array (that we published as a letter in [72]), various size arrays were developed including 2x4, 4x4, and 8x8. These arrays have been fabricated, and are shown in Figure **3.12**. Rogers RT/duroid 5880 substrate with relative dielectric constant of 2.2, loss tangent of 0.0009, and thickness of 0.38 mm was utilized for the microstrip substrate, while the same substrate, however with a thicker thickness of 1.58 mm was used for the cavity substrate in all designs. Standard solder cup SMA connector was employed to launch the microwave signal to the feed network in each case. The two substrates were stacked up by soldering the cavity top metal to the top microstrip substrate. Proper alignment and stacking of the two substrates are imperative to achieve the required performance.

3.5.1 **Return Loss Performance and Fractional Bandwidth**

The various fabricated cavity-backed patch arrays were tested using an Agilent E86386 network analyzer to inspect the return loss performance. Figure **3.13** shows the measured return loss of the different sized arrays. The 2x2 sub-array exhibits a fractional bandwidth of 10%, while the larger arrays exhibits wider fractional bandwidth of 12%, 11.5%, and 13% for the 4x4, 4x8 and 8x8 array respectively.



(a)

(b)

(c)

(d)

Figure 3.12 Picture of the fabricated SIW cavity backed patch arrays. (a) 2x2 array. (b) 2x4 array. (c) 4x4 array. (d) 8x8 array.

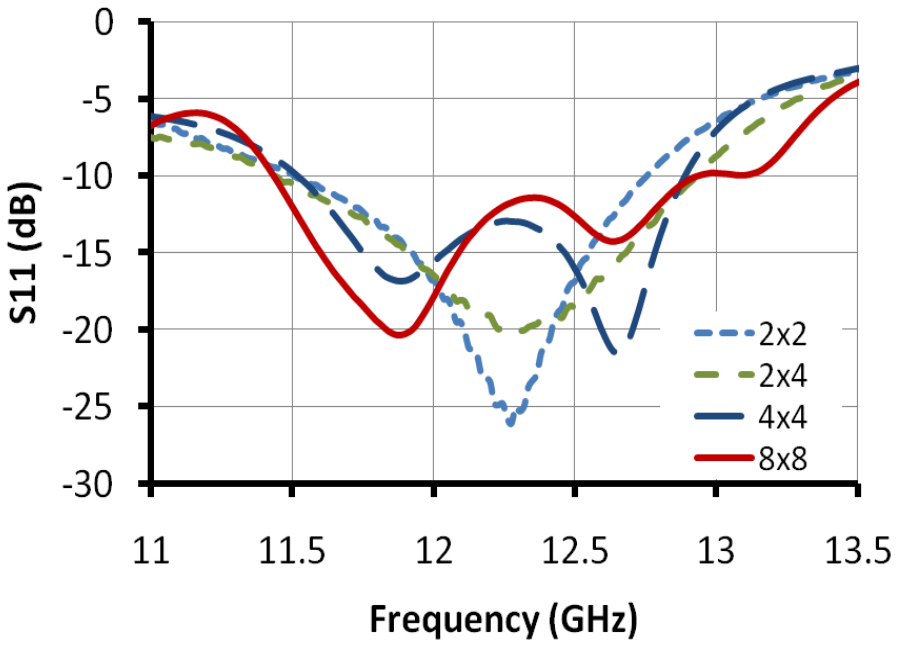
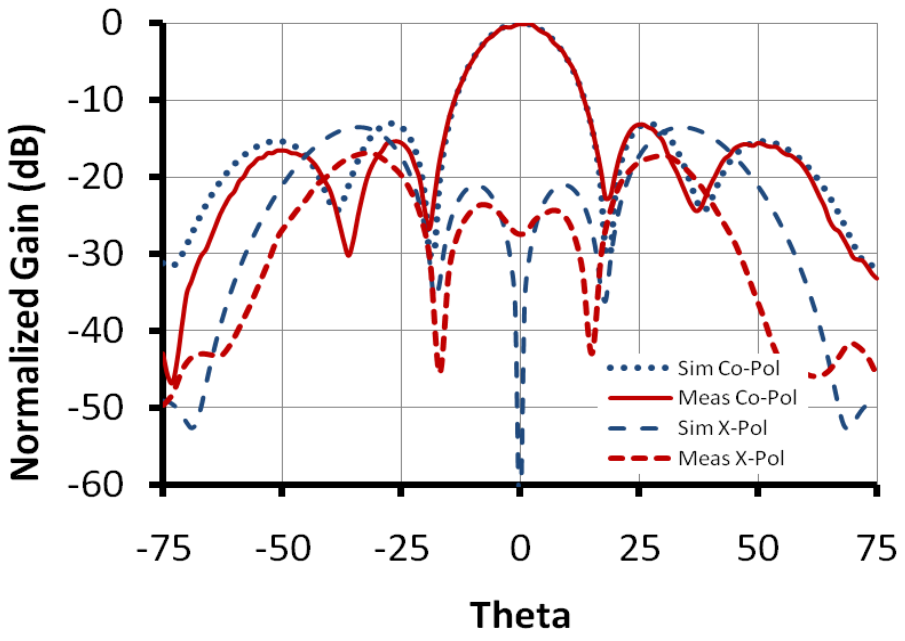


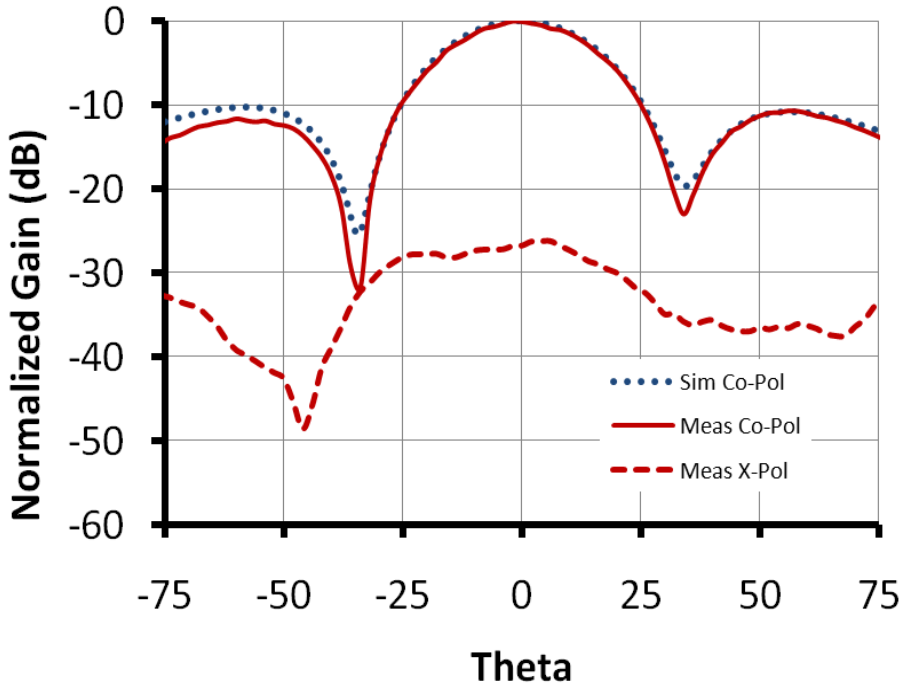
Figure 3.13 Measured reflection coefficient performance of the different SIW cavity-backed patch arrays.

3.5.2 **Radiation Pattern**

The simulated and measured normalized far-field antenna gain patterns at 12.5 GHz are shown in Figure **3.14**, 15, and 16 for the H-plane and E-plane cuts of the 2x4, 4x4, and 8x8 arrays, respectively. Simulated and measured co-polarization data are mostly in good agreement except of some side lobe discrepancies that could be related to a slight airgap stacking problem. For the 2x4 array, the measured side-lobe level is about -11 dB, while the cross-pol is better than -25 dB at broadside, as shown in Figure **3.14**. While, for the 4x4 array, the side-lobe level is better than -12 dB and the cross-pol is better than -30 dB at the broadside direction, as shown in Figure **3.15**. Finally, for the 8x8 array, the measured side-lobe level is -12 dB (similar to the 4x4 array), while the cross-pol is -23 dB (relatively inferior to the 4x4 array), as shown in Figure **3.16**.

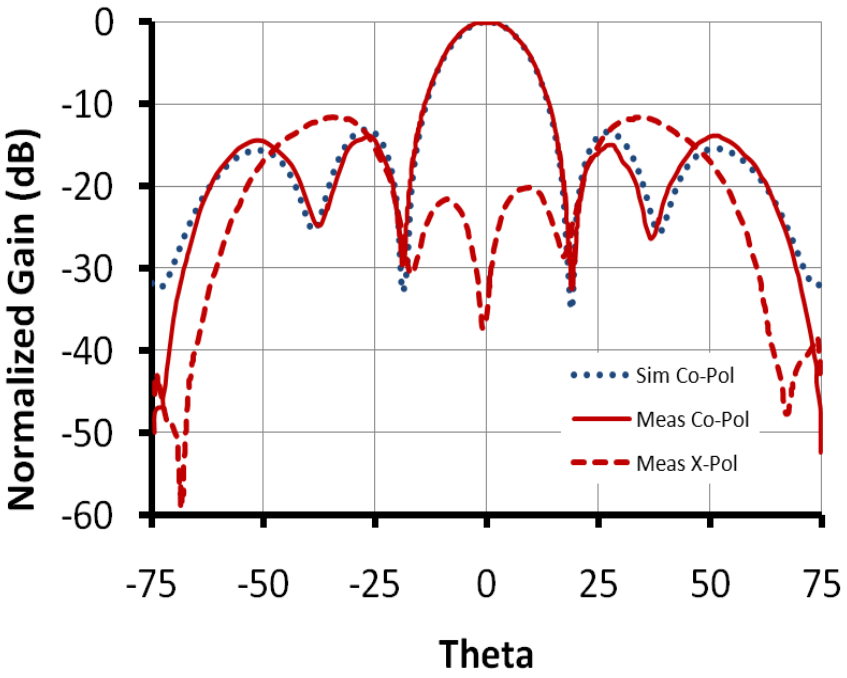


(a)

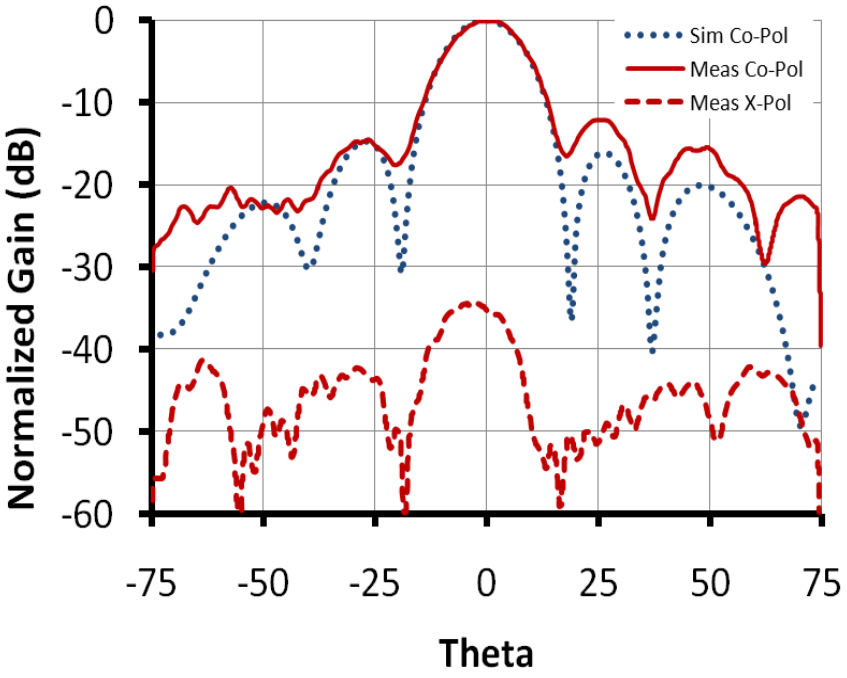


(b)

Figure 3.14 Normalized radiation pattern of the 2x4 array measured at 12.5 GHz. (a) H-Plane. (b) E-Plane.

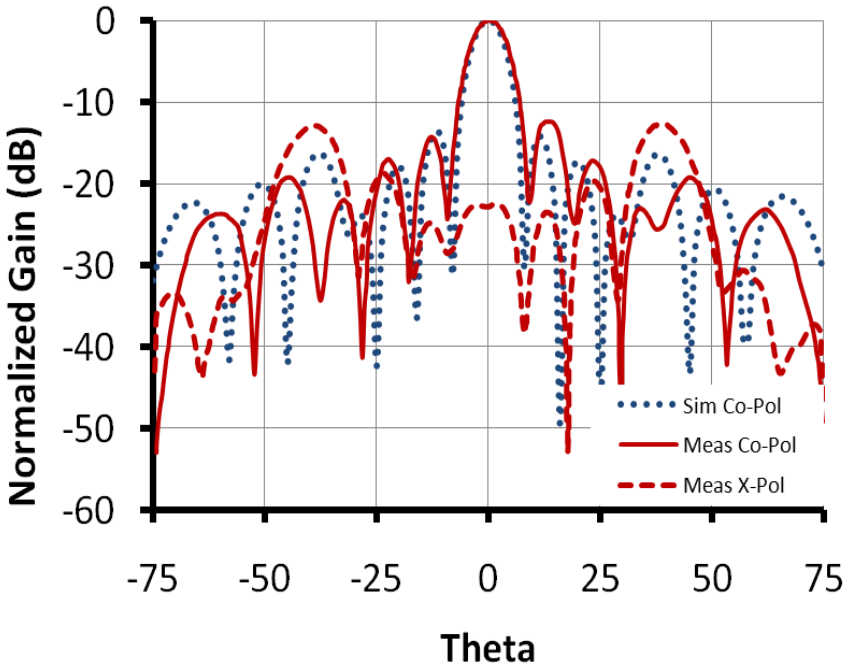


(a)

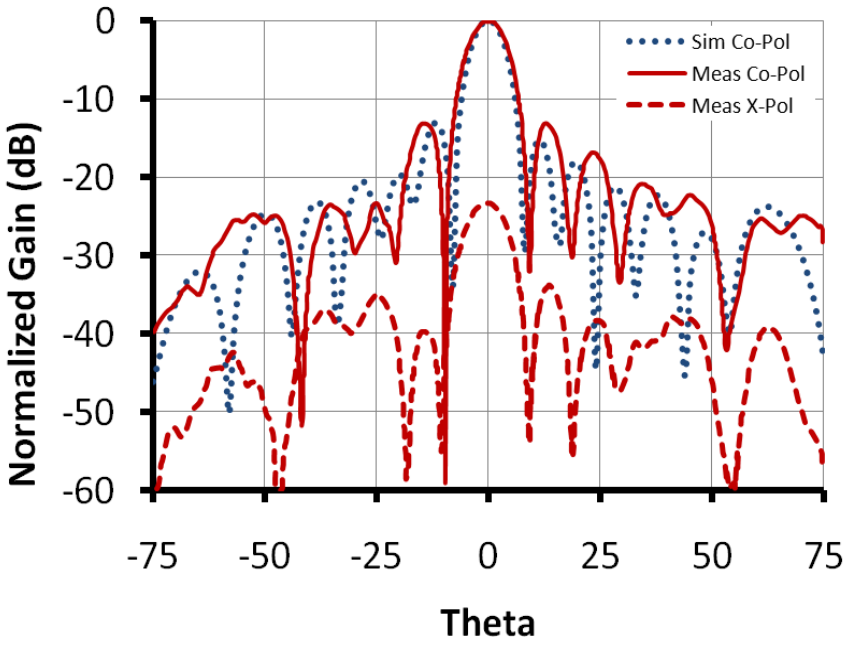


(b)

Figure 3.15 Normalized radiation pattern of the 4x4 array measured at 12.5 GHz. (a) H-Plane. (b) E-Plane.



(a)



(b)

Figure 3.16 Normalized radiation pattern of the 8x8 array measured at 12.5 GHz. (a) H-Plane. (b) E-Plane.

3.5.3 **Gain and Efficiency Performance**

The measured gain versus frequency is shown in Figure **3.17** for the different arrays. Clearly, the relatively small arrays exhibit an almost flat gain over the 12.2 GHz to 12.7 GHz band, while the relatively larger arrays have some gain ripples which have not been seen in our numerical simulation. We attribute this gain ripples to airgaps in the multilayer structure. However, it is believed that the assembly problem could be minimized by using a special prepeg epoxy, as recommended by Rogers Corp., instead of just soldering or bolting the stack together.

Table **3.3** summarizes the measured characteristics of the different sized arrays. Relatively slight differences between the measured gain results and the predicted ones from the simulation (listed previously in Table **3.2**) can be seen. For instance, the simulated gain of the 8x8 array was expected to be 24.7 dBi at 12.5 GHz, however, only a gain of 24 dBi at 12.5 GHz was measured, a noticeable drop by 0.7 dB from the numerical estimates at band center. Based on the single element gain of 8.0 dBi (at 12.5 GHz), we ideally expect about 26.0 dBi (at 12.5 GHz) gain for the array of 8x8 elements. However, the measured actual gain is 24 dBi (at 12.5 GHz). That leads to our estimate of 2 dB loss due to feed losses. Table **3.4** summarizes the losses of the different components we have utilized in the divider, leaving 0.5 dB of unaccounted losses that could be attributed to the assemblage of the structure.

Another problem could be seen for the gain as a function of frequency where gain variations are observed over the band, at some frequencies the gain dropped by more than 1 dB, which could be related again to the airgap problems.

In summary, the efficiency has exceeded 70% for all cases except for the 8x8 case, where only 50% has been achieved. This noticeable efficiency drop for the 8x8 array is related to the excessive losses associated with the relatively large feed network and the stacking problem we encountered. However, it is essential to significantly reduce the feed network losses. Therefore, waveguide feed networks with lower loss would be implemented to retain the efficiency for such large arrays and will be investigated in Chapter 4.

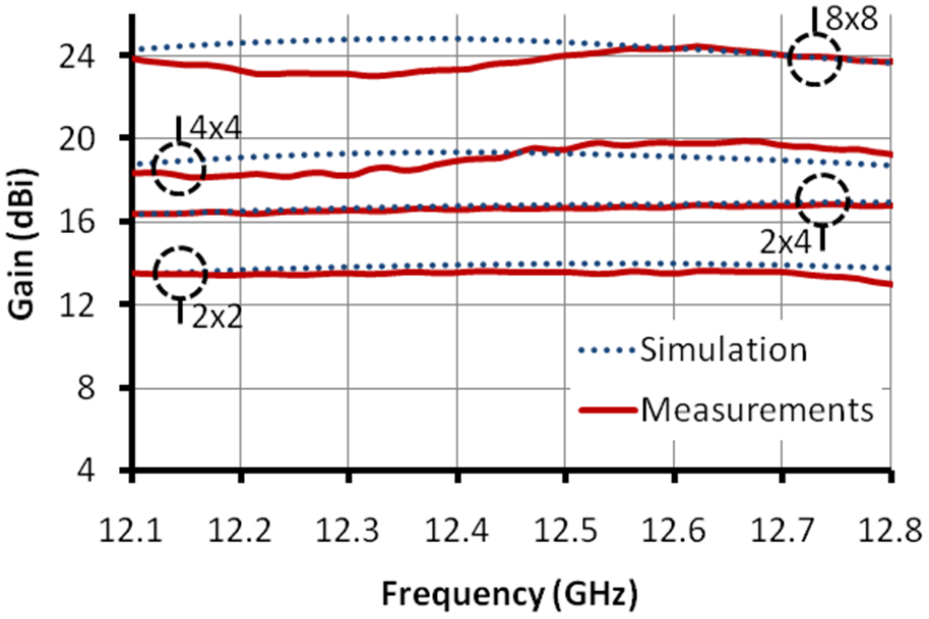


Figure 3.17 Measured gain versus frequency of the different sized arrays.

Table 3.3 Measured performance summary of the different sized SIW cavity-backed arrays at 12.5 GHz

N	Aperture Size (mm^2)	FBW	Gain (dBi)	Aperture Efficiency	SLL (dB)	Cross-Pol (dB)
2x2	38x38	10.0%	13.60	73%	-12	-21
2x4	38x76	12.0%	16.65	73%	-11	-25
4x4	76x76	11.5%	19.46	70%	-12	-35
8x8	152x152	13.0%	24.00	50%	-12	-23

Table 3.4 Summary of losses in the various feed components of the micrsotrip-fed 8x8 array

Component	Loss (dB)
Microstrip Feed Loss (8x8)	1.3
SMA Input Connector	0.2
Unaccounted Losses	0.5

3.6 Conclusion

The proposed SIW cavity-backed arrays consist of a stack of two substrates: the top substrate for the patches and their microstrip feed network and the bottom one for the SIW cavities. The top microstrip substrate should be kept thin in order to impede surface wave propagation and minimize the associated feed network losses. Meanwhile, the bottom cavity substrate should be relatively thick for bandwidth enhancement. A design chart for the basic 2x2 sub-array has been presented and used with a modular design approach to realize larger arrays. The proposed SIW cavity-backed arrays outperform both the thick microstrip and suspended arrays in terms of gain and aperture efficiency. The SIW structure has a comparable performance to the cavity-backed suspended arrays and the conventional metalized cavity-backed arrays, but with a much lower fabrication cost. Various SIW array prototypes have been fabricated and experimentally tested. The fabricated structures, as predicted, have very good radiation characteristics, enhanced bandwidth, and high aperture efficiency up to 4x4 size arrays. But, once we get to arrays with 8x8 elements, significant gain drop was noticed. The 2 dB gain drop (from its theoretical gain value) for the 8x8 array is related to excessive feed loss, and assembly problems. For further performance enhancement, waveguide feed networks could be utilized to substantially lower the dominant loss contributor; i.e. the feed loss and improve the efficiency of large arrays. Meanwhile, stacking more patches could be employed to further widening the operating bandwidth -- if needed.

Chapter 4 SIW Cavity-Backed Patch Array of SIW Feed

It was concluded in Chapter 3 that large arrays with 64 elements or more will suffer significant loss, which is not acceptable. Substrate-integrated waveguide feed is investigated here as an alternative feed topology to lower such feed loss. The long feed lines will be replaced by SIW lines, while microstrip lines will be used to feed small sub-arrays like the 2x2 or even the 2x4. This strategy is based on the fact that small size arrays have demonstrated over 70% efficiency, as have been shown in Chapter 3. Use of SIW feeds with significantly lower loss should improve the overall antenna efficiency. For demonstration, three different sized arrays are analyzed and experimentally tested of 4x4, 4x8 and 4x16 elements. Performance of the arrays is demonstrated and is compared to the corresponding microstrip-fed arrays.

4.1 Waveguide Feed

It is well known that the losses of waveguides (either circular or rectangular) are far less than the microstrip lines [73-74]. This lower loss essentially originates from the nature of the waveguide, as a closed guiding structure, compared to the microstrip which is an open guiding structure, where the electromagnetic mode of waveguide operation enjoys one order of magnitude lower loss.

Replacing the microstrip feed lines whenever possible by waveguides will definitely lower the feed loss and thus increases the antenna's radiation efficiency. For DBS arrays several authors have utilized waveguide feed networks to achieve better overall antenna performance. For instance, Shahabadi et. al in [18] utilized the metalized feed network, shown in Figure **4.1**, to feed a 2x16 array of microstrip patches. The overall feed loss of their waveguide structure was only 0.2 dB. Similar waveguide feed network was developed by Kimura et. al in [75] to feed their slotted waveguide antenna as shown in Figure **4.2**.

On the other hand, substrate-integrated waveguide recently have been used in DBS arrays to avoid the fabrication complexity of conventional metalized waveguide feed networks. Figure **4.3** shows the SIW divider developed by Yang in [37] to feed his slotted DBS array. The losses of the 1-32 divider is just about 0.7 dB. Meanwhile, Busuioc et. al. in [35] developed a 1-4 SIW divider to feed their 4x8 patch array, as shown in Figure **4.4**, to replace the waveguide feed they developed before in [18]. They reported that upon replacing the solid waveguide feed by SIW version the loss is just 0.5 dB which is expected because of the dielectric loss associated with the SIW feeds.

Figure 4.1 Waveguide feed network utilized by Shahabadi, et. al in their DBS microstrip patch array [18].

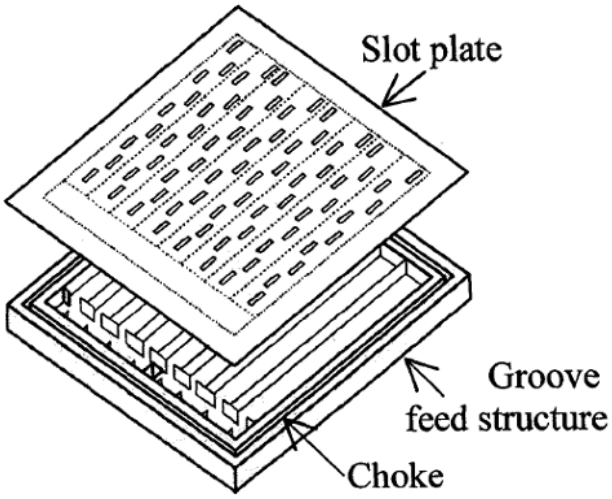


Figure 4.2 Waveguide feed network utilized by Kimura, et. al in their slotted waveguide antenna array [78].

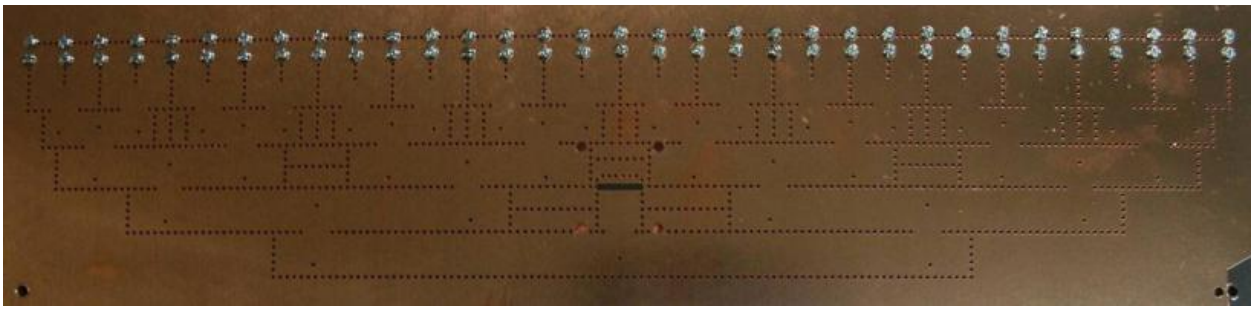


Figure 4.3 Substrate-integrated waveguide feed network utilized by Songnan, et. al in their cross-slotted waveguide antenna array [37].

Figure 4.4 Substrate-integrated waveguide feed network utilized by Busuioc, et. al in their microstrip patch antenna array [35].

4.2 Developed Waveguide Feed Network

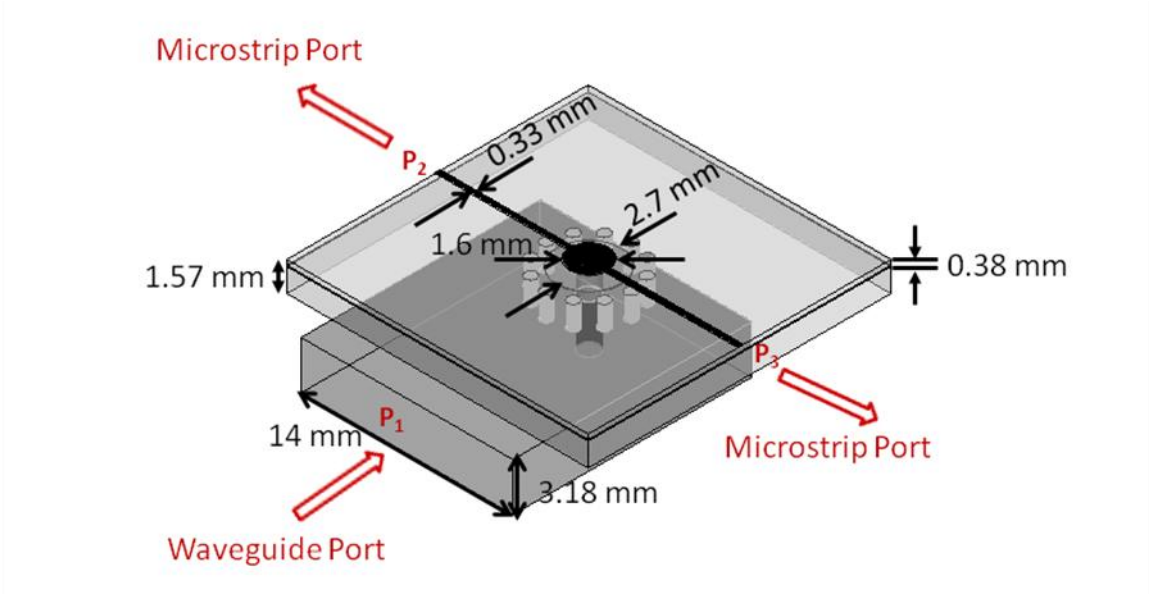
We have developed a full waveguide divider feed network assuming that the waveguide is filled with dielectric to include the dielectric losses in our calculations. Initially, perfect electric boundary conditions were enforced on the waveguide boundaries to speed up computation. Later, the assumed perfect electric walls of the divider have been replaced by via holes.

4.2.1 **Waveguide to Microstrip Transition**

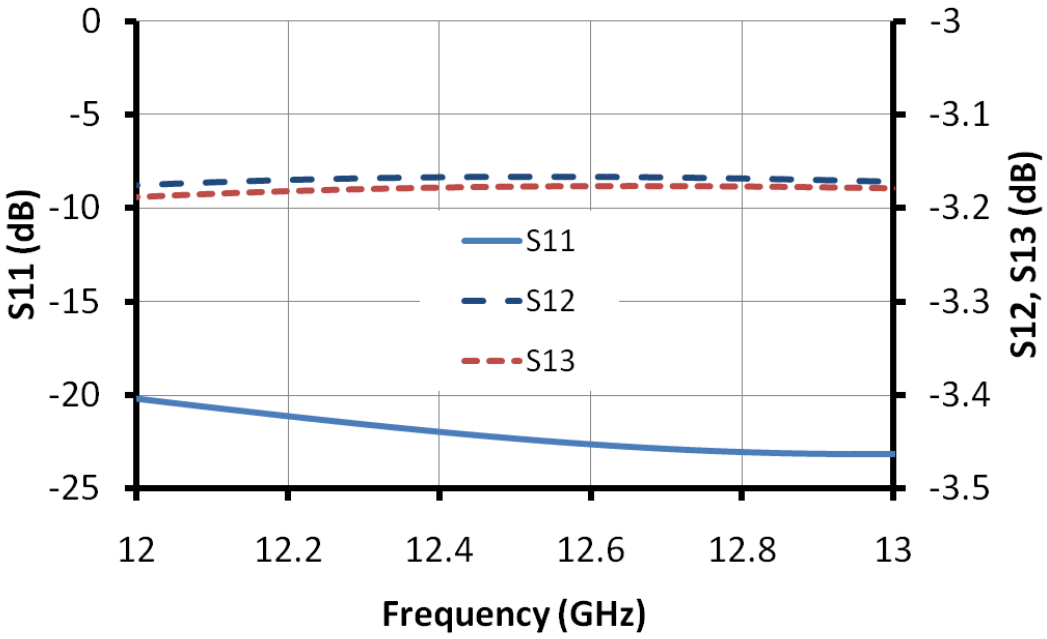
As mentioned before, the proposed array has a mixed microstrip-waveguide feed topology where the waveguides have replaced only the long microstrip lines, while on the sub-array level we still have microstrip feeding lines. Therefore, it was necessary to develop a transition from the waveguide feeding lines to the microstrip lines. Figure **4.5**(a) shows the proposed transition. Basically, the transition consists of three substrates; a bottom substrate that contains the waveguide feed, a middle substrate that contains an integrated coaxial line, and a top substrate where the microstrip line is printed. A probe is going through the three substrates to couple the energy from the waveguide to the microstrip line. Similar transition has been developed before by Busuioc et. al. in [35], however in difference to [35] we have surrounded the probe by many platted via holes to minimize the associated radiation loss. The proposed transition has been modeled using HFSS and its simulated S-parameters are shown in Figure **4.5** (b). The proposed transition exhibits only a 0.2 dB insertion loss compared to 0.4 dB in [35], which demonstrates that the via holes works well to achieve lower losses of the transition.

4.2.2 **Input Waveguide Transition**

In order to excite the feed network several topologies could be used. One possibility is to use a standard waveguide transition and then couple the transition to the feed network using an iris. Figure **4.6**(a) shows an example for such a transition where WR75 standard waveguide was assumed for the input guide. The insertion loss of this kind of transitions is very low. For instance, the simulated insertion loss of the modeled transition is about 0.1 dB in the DBS band of interest, as shown in Figure **4.6**(b).

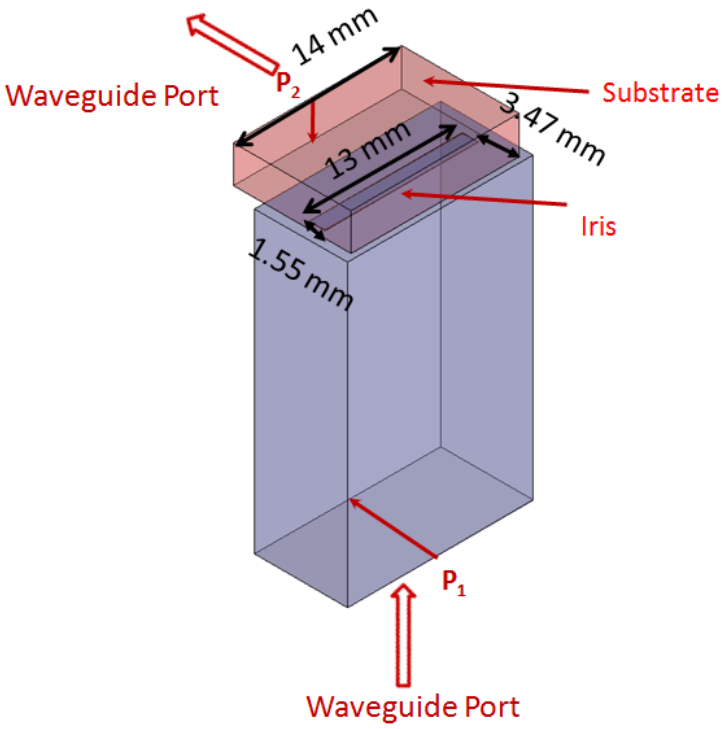


(a)

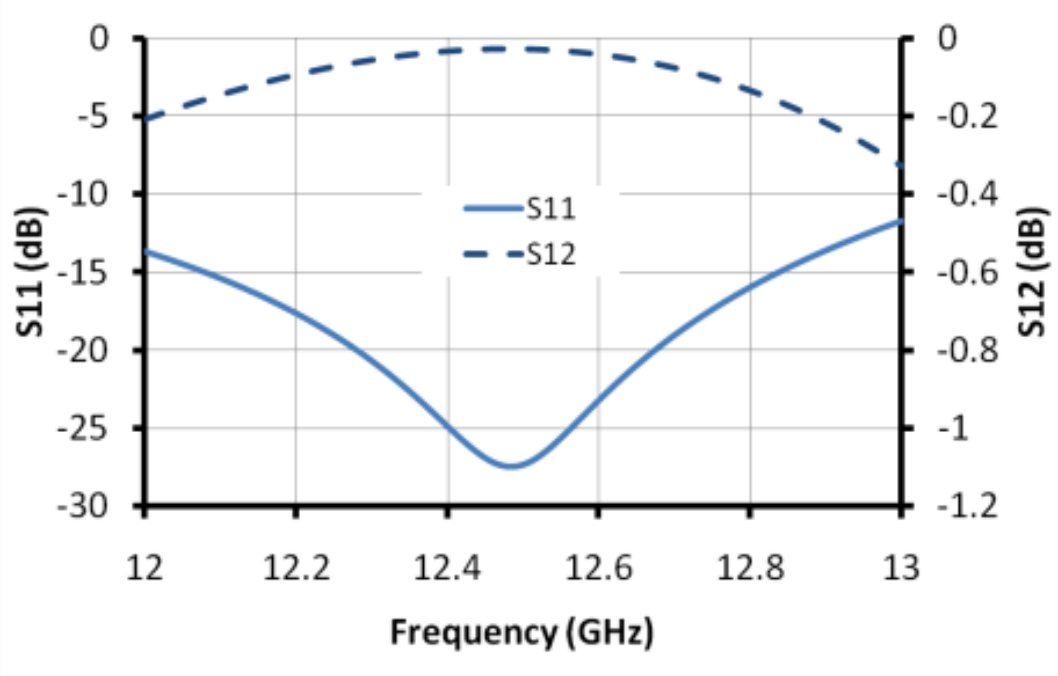


(b)

Figure 4.5 Waveguide to microstip transition (all substrates are assumed to have ε_r of 2.2). (a) HFSS model. (b) Simulated S-parameters.



(a)



(b)

Figure 4.6 Input waveguide transition (substrate is assumed to have ε_r of 2.2). (a) HFSS model. (b) Simulated reflection response.

4.2.3 **Input CPW Transition**

An alternative waveguide transition was suggested by S. Lin et. al. in [76], is to excite the substrate integrated waveguide by a coplanar transition, as shown in Figure **4.7**(a). The transition has the advantage of being co-planar to the structure in difference to the previous waveguide transition which will be feeding the structure from the back. However, the insertion loss of the CPW transition is expected to be relatively higher than the waveguide transition because of the CPW associated radiation loss. For instance, the CPW transition designed for Ku band frequency theoretically exhibits about 0.4 dB insertion loss, as shown in Figure **4.7**(b) (S. Lin in [76] reported about 0.7 dB measured insertion loss for a similar transition designed to operate from 8 to 10 GHz).

4.2.4 **Waveguide Corner**

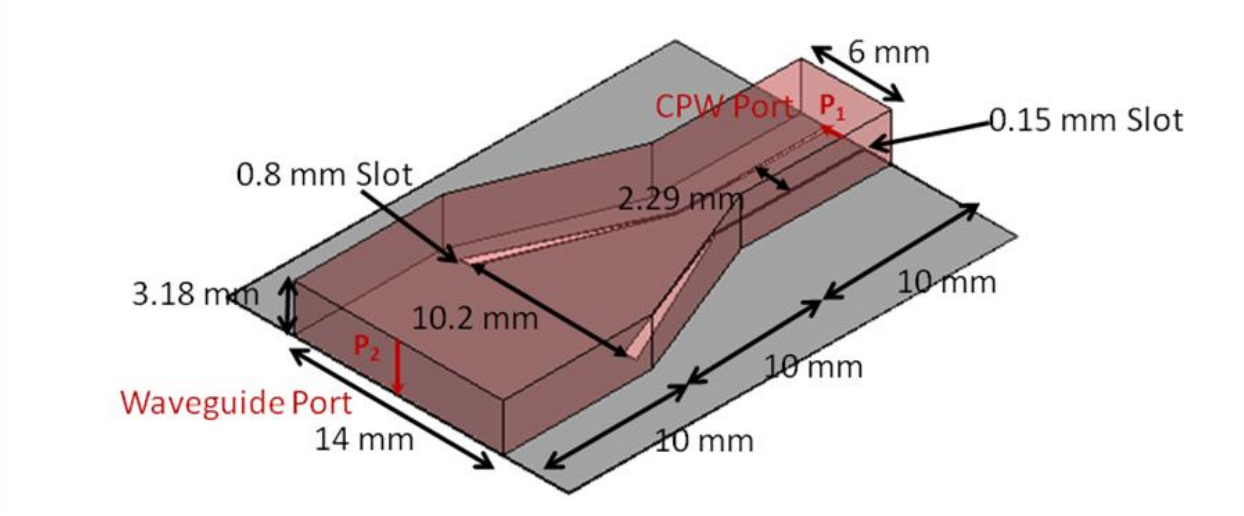
In building the waveguide feed network, we definitely need corner transitions. Figure **4.8** shows a conventional mitered corner and a proposed corner transition, where a via hole was placed at the coroner instead of mitering the bend (similar to [37]). The insertion loss of the proposed corner transition is less than 0.1 dB, as shown in Figure **4.8**(c), compared to 0.08 dB for the mitered corner.

4.2.5 **Waveguide T-Junction**

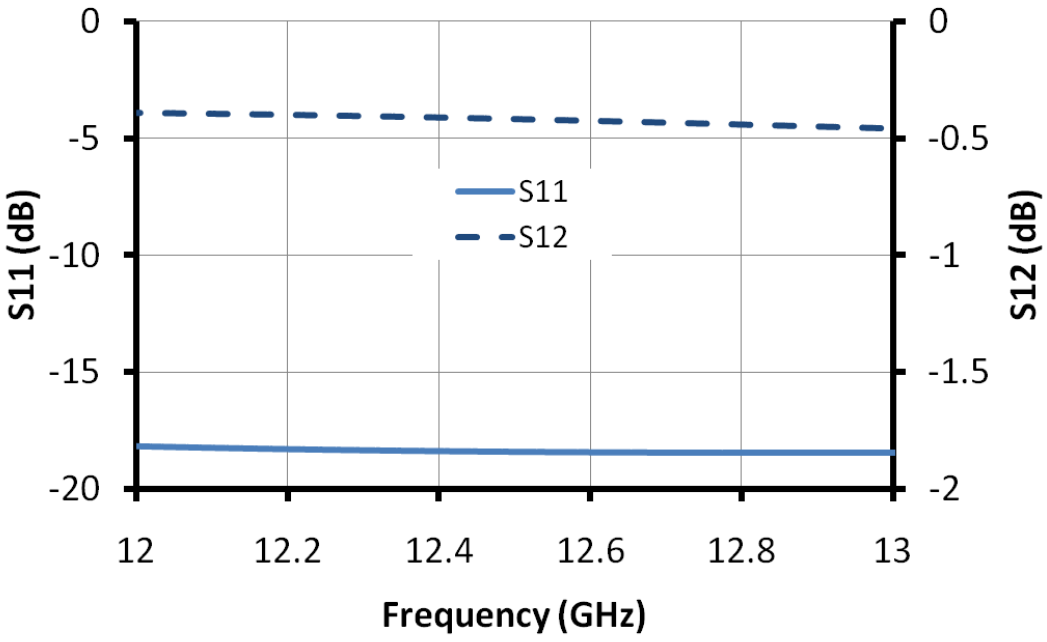
T Junctions are also essential building blocks in building the waveguide dividers. Figure **4.9**(a) shows an HFSS model of the utilized T-Junction, where via holes have been placed to substitute the diaphragm and the septum transitions. Here we have developed a T-Junction for equal power split, however arbitrary split ratio T-Junctions could be realized, as described in [77]. The theoretical insertion loss of the developed T-Junction is less than 0.05 dB, as shown in Figure **4.9**(b), which is very close to that measured (0.03 dB) by S. Yang et. al. for a similar T-Junction in [77].

4.2.6 **Waveguide Y-Junction**

In our feed network, we needed also to use Y-Junctions, as shown in Figure **4.10**(a). The reason for that will appear later when we demonstrate the dual-polarized array (Chapter 5), where a twin interleaved feed will be used. Figure **4.10**(b) shows the simulated reflection response of the transition, where less than 0.2 dB insertion loss is exhibited by the Y-Junction. The developed Y-Junction will be used later in this chapter to feed a 4x4 SIW-fed array.

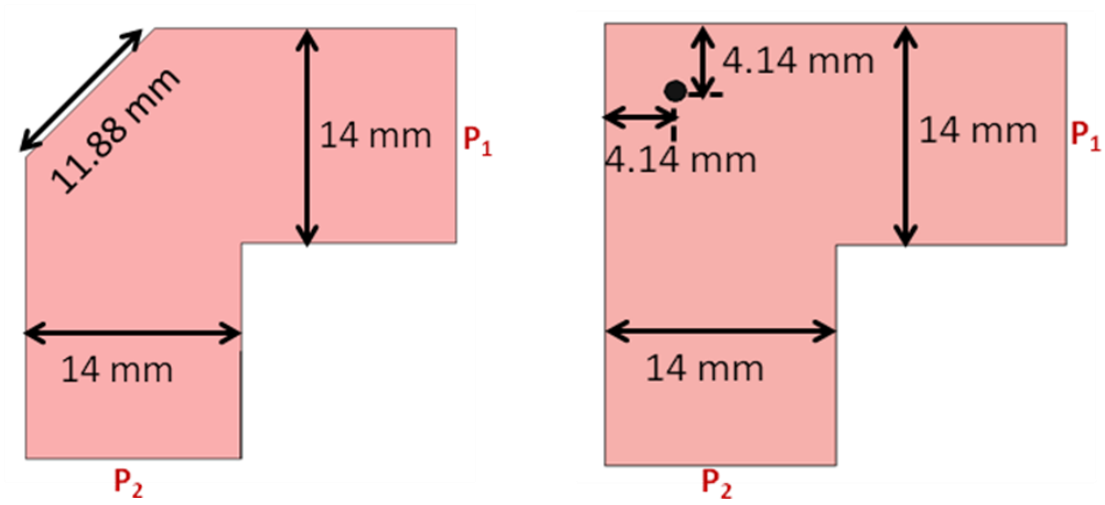


(a)

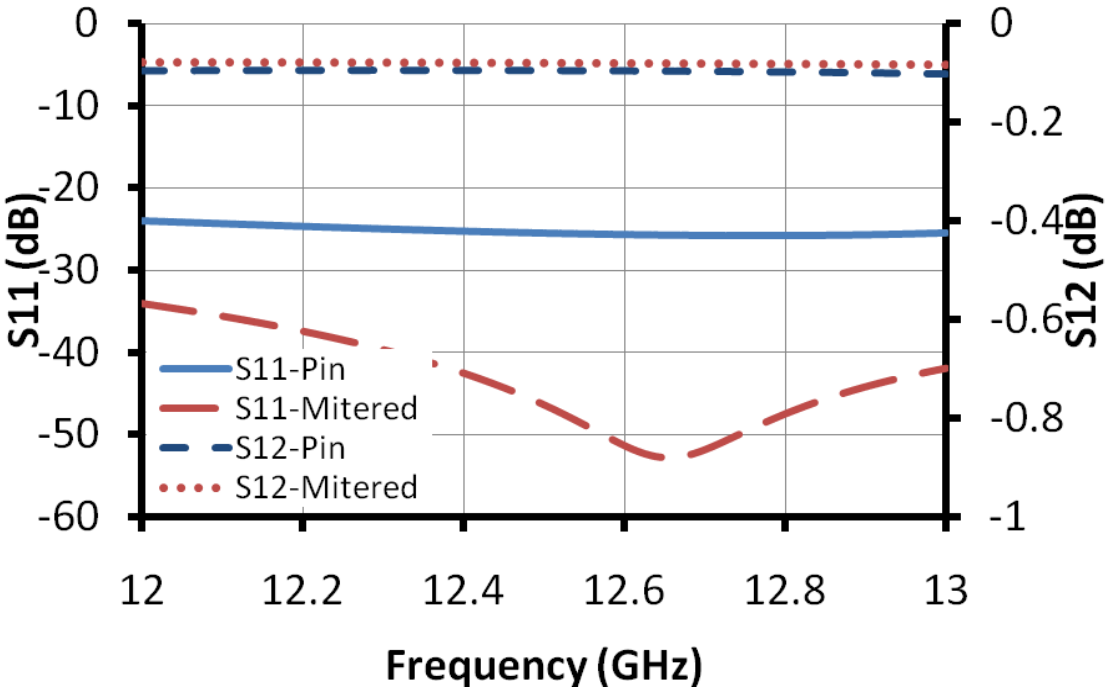


(b)

Figure 4.7 CPW to waveguide transition (substrate is assumed to have ε_r of 2.2). (a) HFSS model. (b) Simulated reflection response.

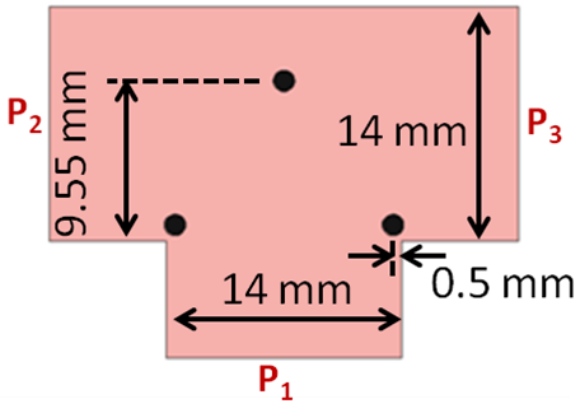


(a) (b)

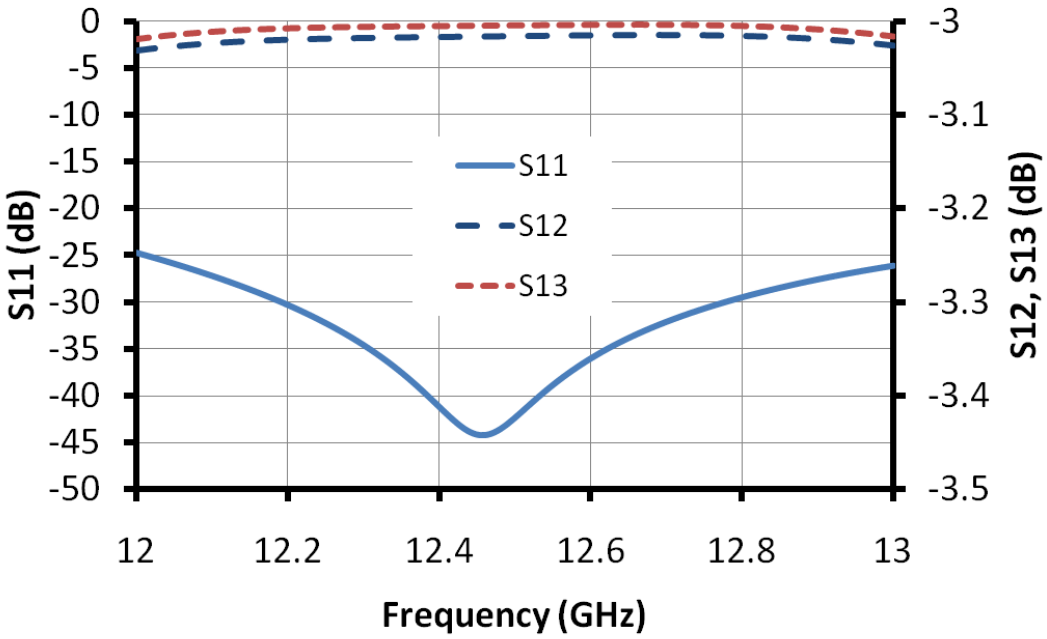


(b)

Figure 4.8 Waveguide corner (assuming ε_r of 2.2 and height 3.18 mm). (a) Mitered corner. (b) Corner with pin. (c) Simulated reflection response.

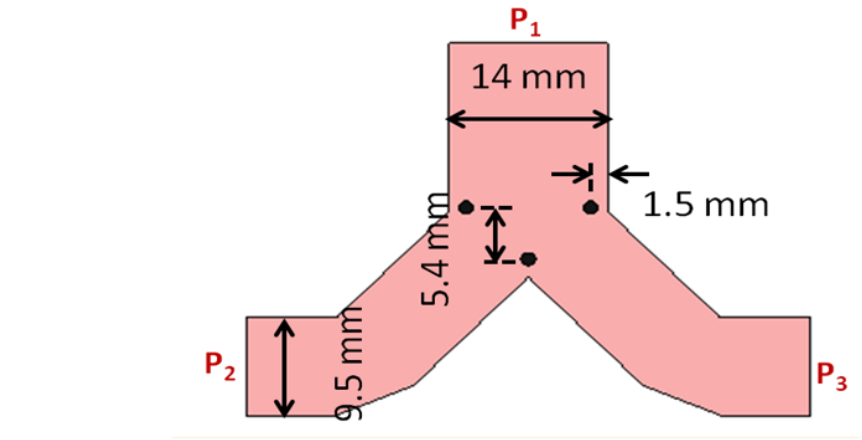


(a)

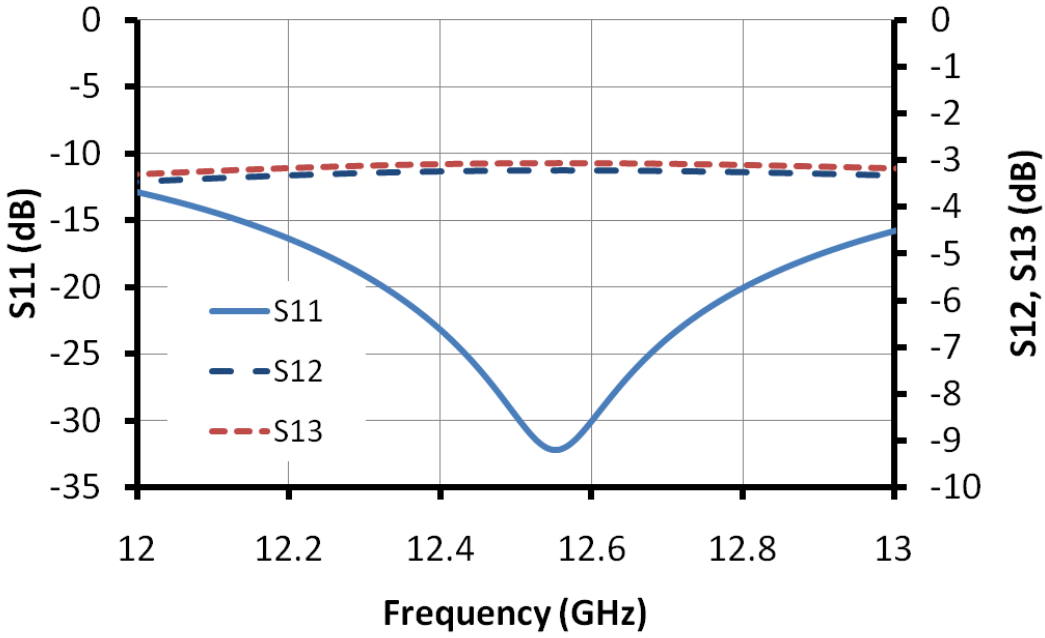


(b)

Figure 4.9 Waveguide T-Junction (assuming ε_r of 2.2 and height 3.18 mm). (a) HFSS model. (b) Simulated reflection response.



(a)

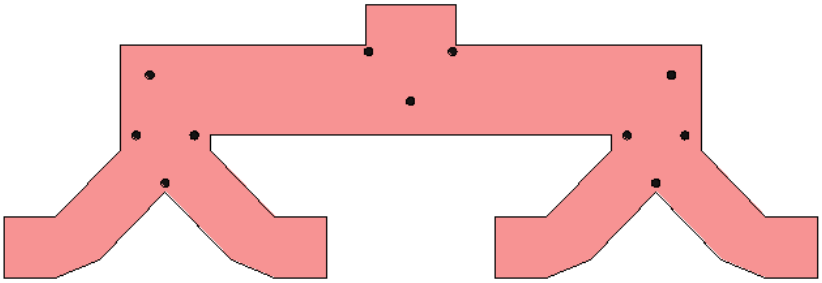


(b)

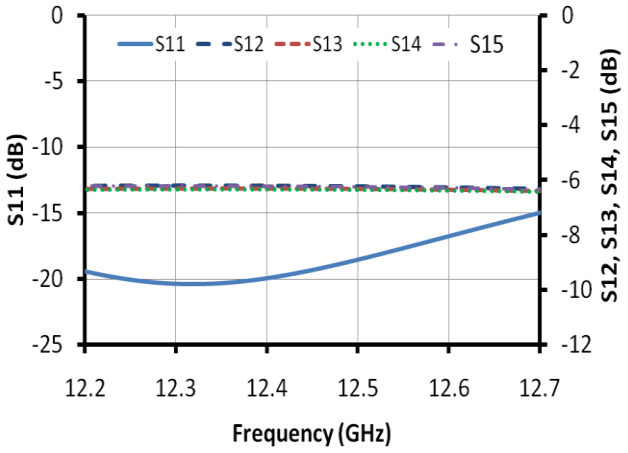
Figure 4.10 Waveguide Y-Junction (assuming ε_r of 2.2 and height 3.18 mm). (a) HFSS model. (b) Simulated reflection response.

4.2.7 **One-to-Four Waveguide Divider**

In this subsection, we show the performance of a one-to-four divider that will be used later to feed a 4x8 SIW-fed array. We have utilized the previously developed components in building the divider, as shown in Figure **4.11**(a). The developed one-to-four divider exhibits about 0.4 dB insertion loss, as shown in Figure **4.10**(b). Meanwhile, the transmission coefficients at the different divider ports are in good phase agreement within 1° difference.



(a)



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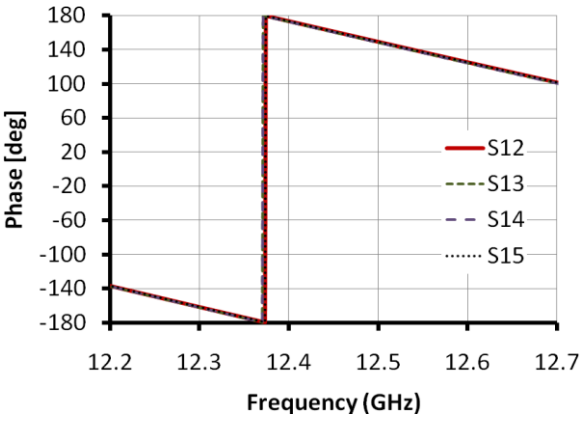


(c)

Figure 4.11 Waveguide one-to-four divider. (a) HFSS model. (b) Simulated magnitude of S-paramters. (c) Simulated phase of S-parameters.

4.3 Microstrip Sub-array

As mentioned before, we will replace only the long microstrip lines by waveguide lines keeping the microstrip feed topology, used before in Chapter 3, on the sub-array level. Figure **4.12** shows the 2x4 microstrip-fed sub-array that will be used in building larger SIW-fed arrays. We have used here opposite feed topology to minimize the space occupied by a single polarization feed network thus accommodate more space, that could be used for staggering dual-feed networks to achieve dual-polarized array, as will be discussed later in Chapter 5.

Figure **4.13** shows the simulated reflection response of the microstrip sub-array, where it covers the required 12.2-12.7 GHz DBS frequency band, exhibiting about 5% fractional bandwidth. On the other hand, the simulated gain patterns of the sub-array are shown in Figure **4.14**. The 2x4 sub-array exhibits less than -11 dB side-lobe level, and less than -30 dB cross-polarization level. The sub-array also exhibits 17 dBi gain at 12.5 GHz.

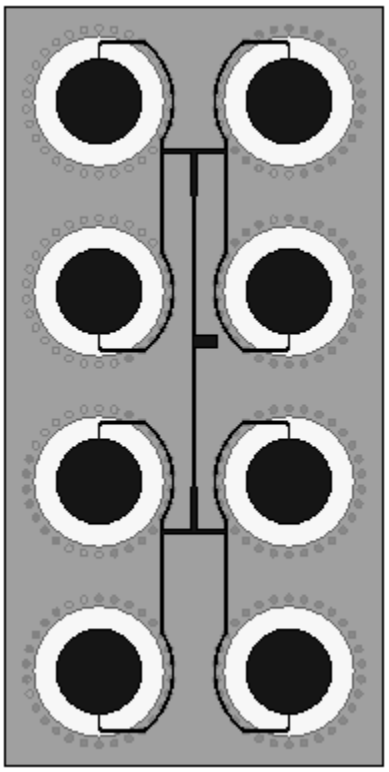


Figure 4.12 Microstrip sub-array of 2x4 elements

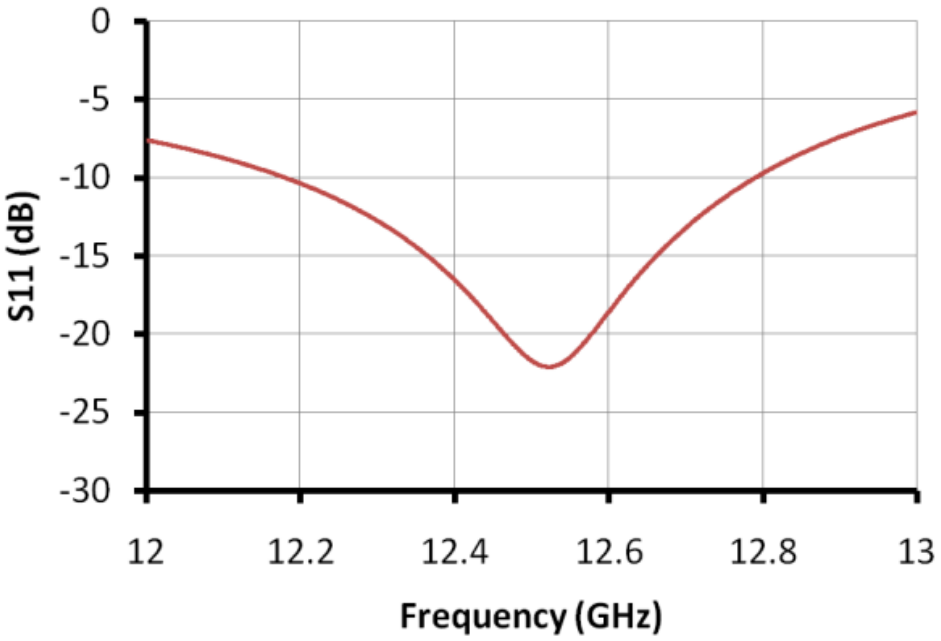


Figure 4.13 Simulated reflection response of the 2x4 microstrip sub-array.

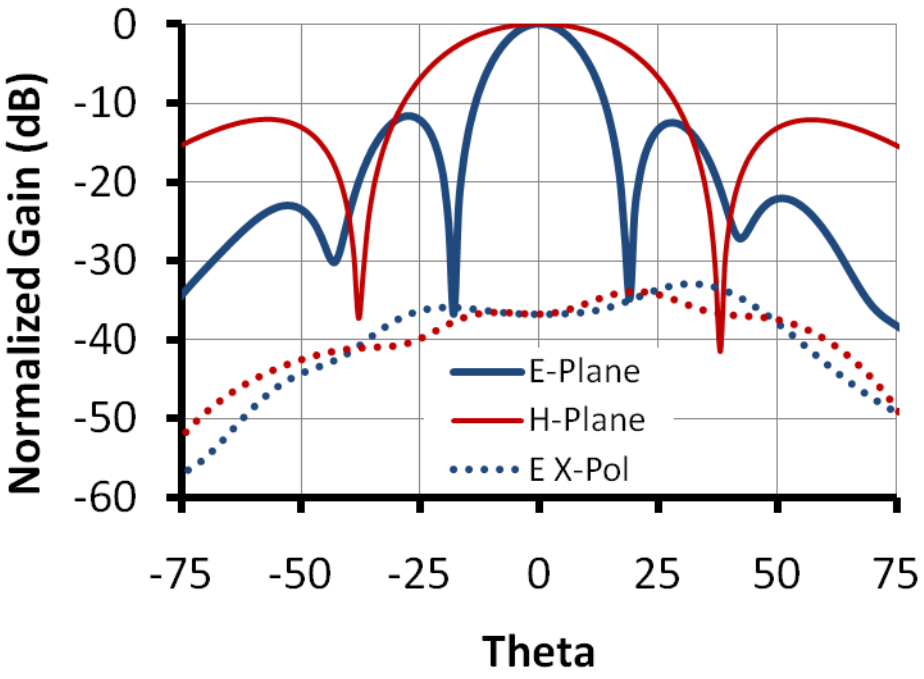


Figure 4.14 Simulated gain patterns of the 2x4 microstrip sub-array.

4.4 4x4 Array

4.4.1 **Array Configuration**

Figure **4.15** shows the proposed SIW-fed 4x4 array depicting the different layers of the structure spaced apart. The structure basically consists of three substrates. Similar to the micrstrip-fed arrays, we have a microstrip substrate where the radiating patch elements are printed along with the microstrip feeding lines on the sub-array level, and a cavity substrate where the SIW cavities are implemented to back the radiating elements. However, in different to the microstrip-fed arrays we have a third substrate "feed substrate" where the SIW feed network is implemented.

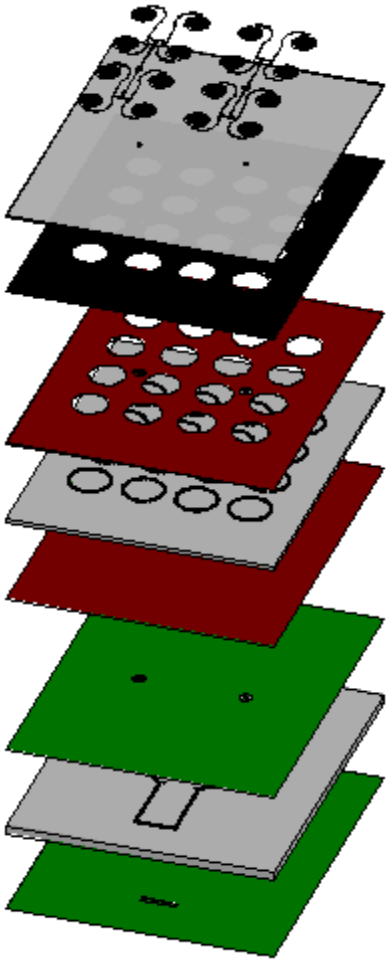
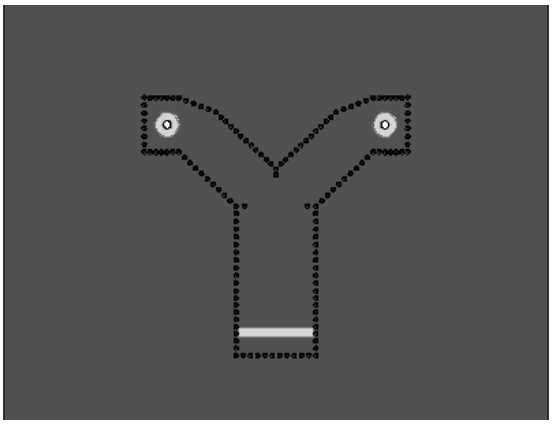


Figure 4.15 Array configuration of the 4x4 SIW-fed array depicting the different layers.

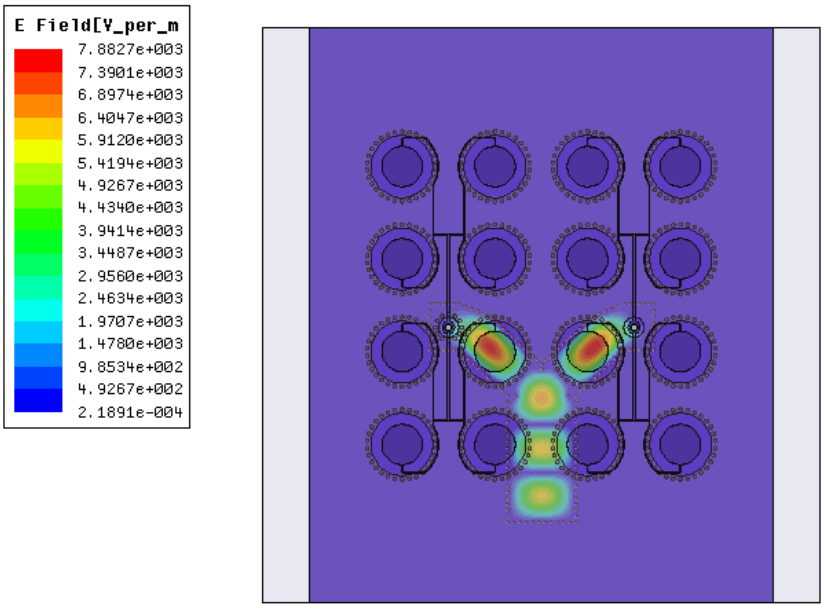
4.4.2 **SIW Divider**

For the 4x4 array, a one-to-two divider shown in Figure **4.16**(a) was designed and implemented to divide the power to the two 2x4 sub-arrays. The divider is being fed by a WR75 waveguide through an opening iris in the lower metal of the feed substrate, as explained before.

Figure **4.16**(b) shows the electric field on the lower surface of the divider simulated using Ansoft HFSS. It is imperative in the divider design to achieve amplitude and phase balance between the divider outputs. In that perspective, diaphragm and septum via holes were added and carefully tuned to achieve that goal.



(a)

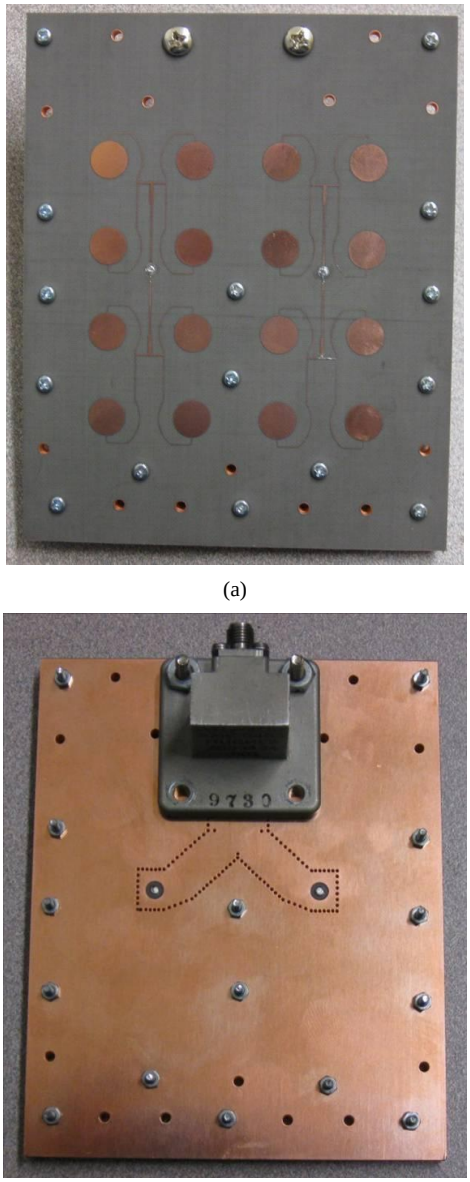


(b)

Figure 4.16 SIW one-to-two divider. (a) HFSS model. (b) Electric field distribution on the lower surface.

4.4.3 **Experimental Results**

The SIW-fed 4x4 array has been fabricated. Picture of the fabricated structure after assemblage is shown in Figure **4.17**. Taconic TLY-5 substrates of dielectric constant 2.2, loss tangent 0.0009, and thicknesses of 3.175 mm, 1.575 mm, and 0.381 mm, have been utilized in the fabrication of the feed, cavity, and microstrip substrates, respectively. Several metal screws have been used to stack the different substrates.



(a)

(b)

Figure 4.17 Picture of the fabricated 4x4 SIW-fed array. (a) Top view. (b) Bottom view.

The fabricated array has been measured. Figure **4.18** shows the measured reflection coefficient of the SIW-fed 4x4 array compared to its simulated results. The array exhibits a good matching performance along the 12.2 -12.7GHz DBS band. The measured return loss is slightly off from the simulated results, however fortunately showed better performance.

Far field antenna measurements have been carried out for the array, as well. Figure **4.19** shows the normalized measured E- and H-Plane gain patterns compared to the simulated ones. Good agreement between the measured and simulated patterns is observed. The array exhibits a side lobe level of -11 dB while the cross polarization level is better than -25 dB.

Finally, the gain versus frequency has been measured as well, as shown in Figure **4.20** for the SIW-fed 4x4 array, and is compared to that of the microstrip-fed corresponding array that was demonstrated before in Chapter3. Obviously, the SIW-fed array exhibits a higher gain. Better than 0.6 dB difference is observed along the DBS band of interest. The higher gain is expected (already have been demonstrated before by many researchers [35, 37]) and clearly validates that the SIW as a low loss feed topology compared to the microstrip feed, yet it is also a low cost one when compared to the conventional waveguide-fed structures.

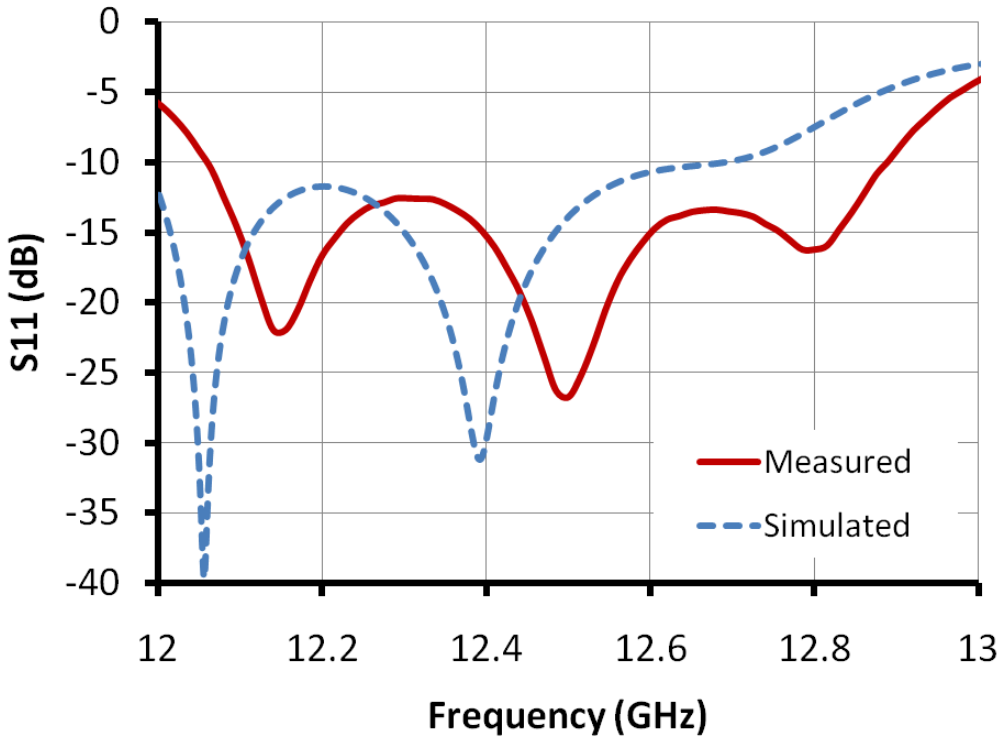
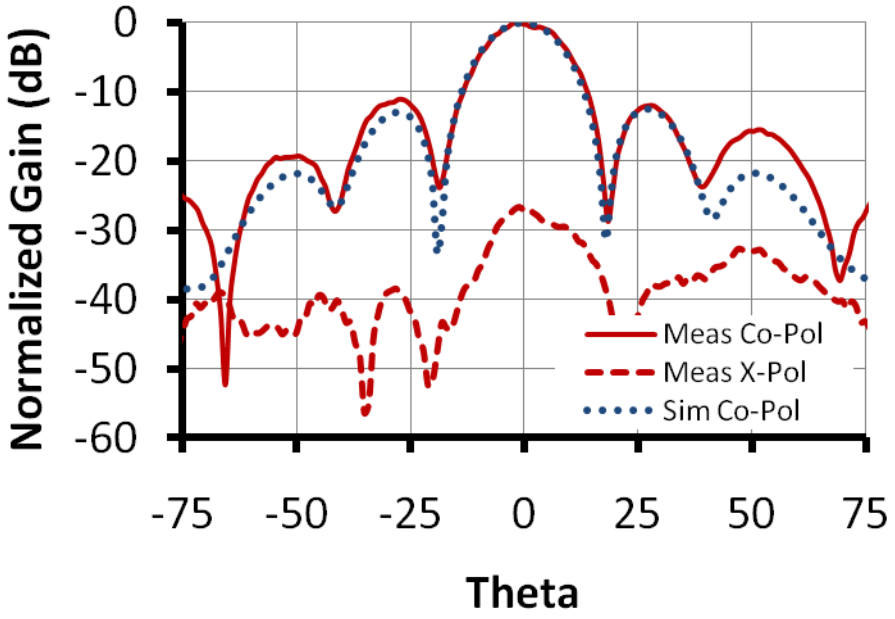
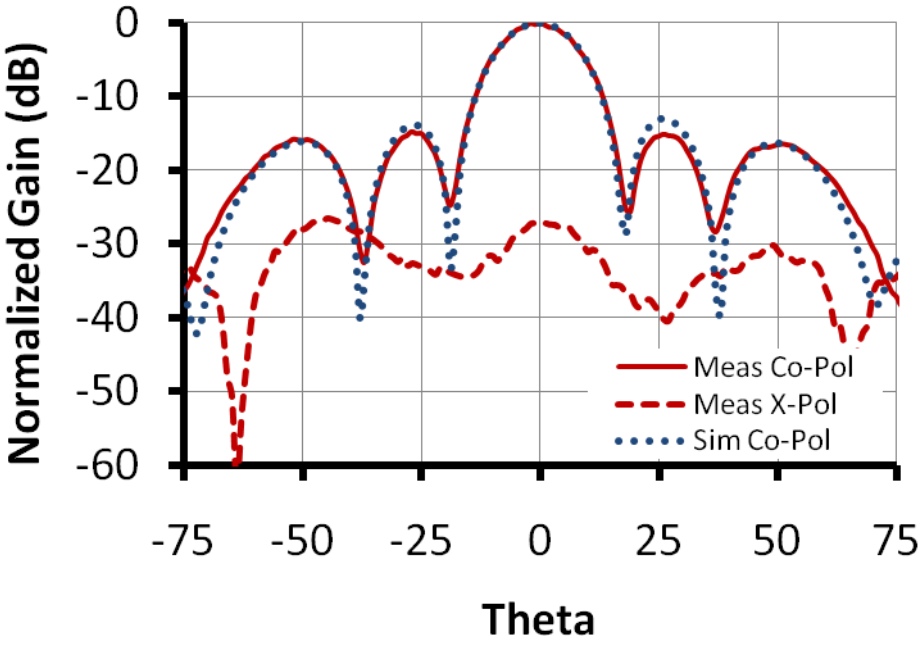


Figure 4.18 Measured reflection response of the 4x4 SIW-fed array compared to simulation.



(a)



(b)

Figure 4.19 Measured gain pattern of the 4x4 SIW-fed array compared to simulation. (a) E-Plane. (b) H-Plane.

Table **4.1** summarize the losses of the various feed components of the SIW-fed 4x4 array based on our previous simulation study of each of them. Given that the single element gain of the circular patch backed by a circular cavity is about 8.6 dBi (at 12.5 GHz), we ideally expect about 20.6 dBi gain (at 12.5 GHz) for the array of 4x4 elements. However, the measured gain of the array at 12.5 GHz is 20 dBi. The 0.6 dB difference between the expected ideal gain and the measured one originates from the losses of the feed network, as listed in Table **4.1**.

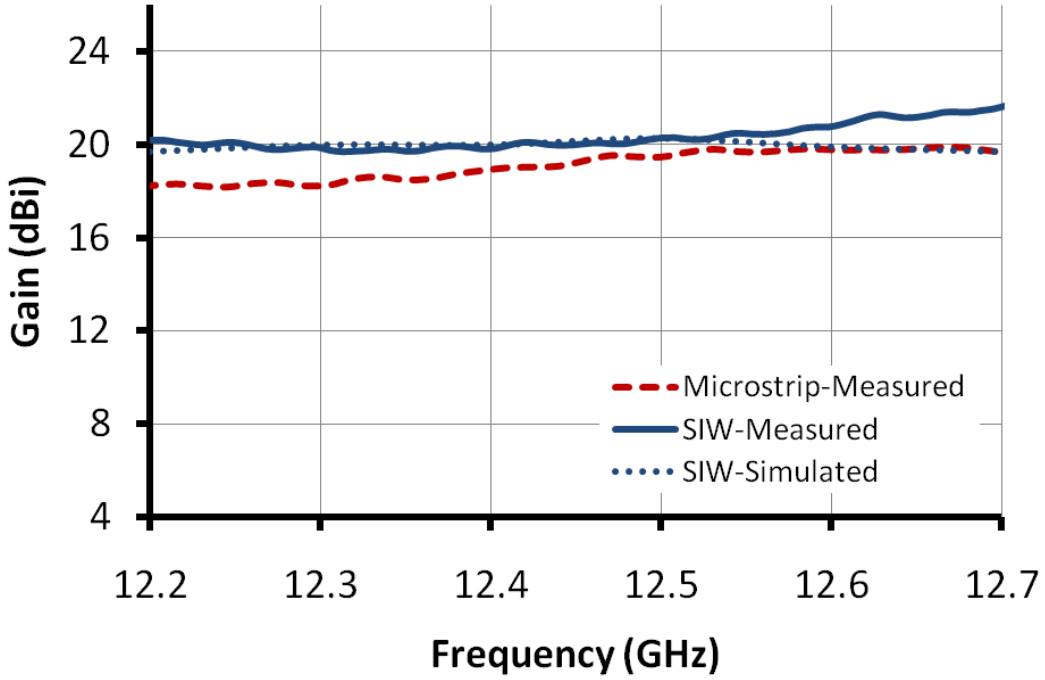


Figure 4.20 Measured gain vs frequency of the 4x4 SIW-fed array compared to the corresponding microstrip-fed array (demonstrated before in Ch3).

Table 4.1 Summary of losses in the various feed components of the SIW-fed 4x4 array

Component	Loss (dB)
Microstrip Feed Loss (2x4)	0.3
Microstrip to Coaxial Transition to SIW	0.2
SIW Feed	0.1

4.5 4x8 Array

4.5.1 **Array Configuration**

Similarly, the SIW-feed topology has been used with larger array of 4x8 elements, as shown in Figure **4.21**. Again the array consists of three substrates; microstrip substrate, cavity substrate and feed substrate.

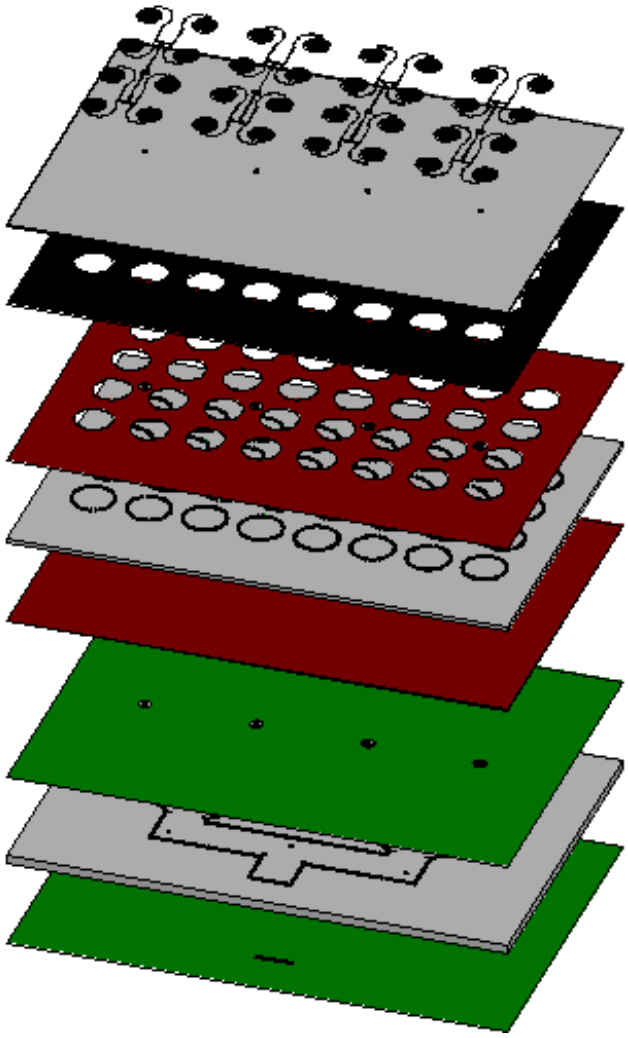
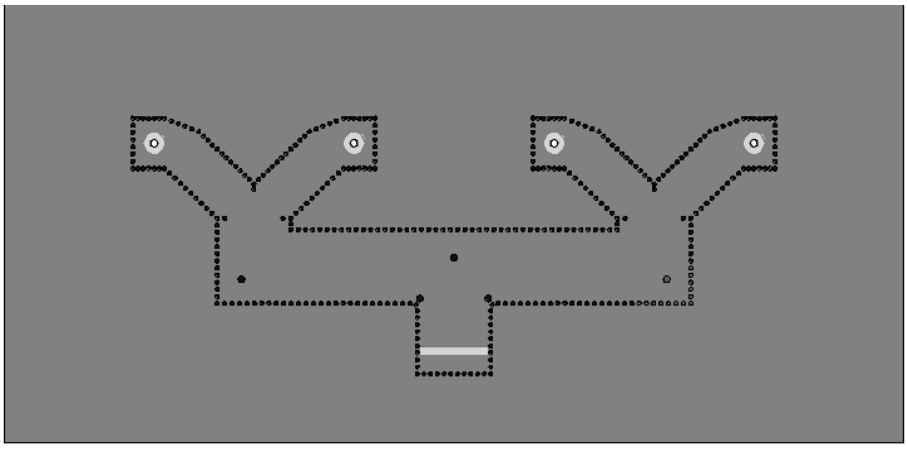


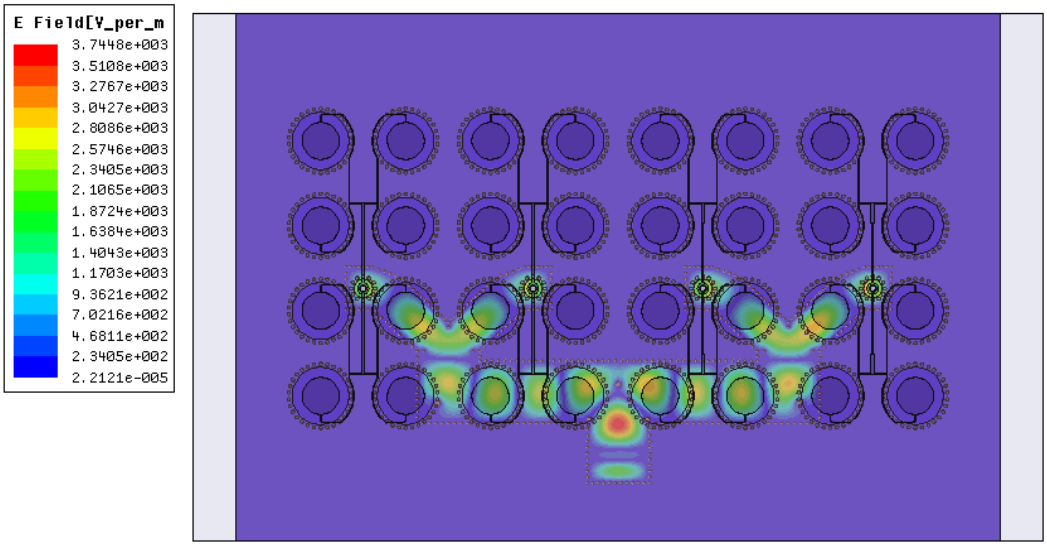
Figure 4.21 Array configuration of the 4x8 SIW-fed array depicting the different layers.

4.5.2 **SIW Divider**

A one-to-four SIW divider is utilized to distribute the energy from the input feeding WR75 waveguide to four 2x4 sub-arrays, as shown in Figure **4.22**(a). The electric field distribution on the bottom surface of the divider calculated using Ansoft HFSS is shown in Figure **4.22**(b).



(a)

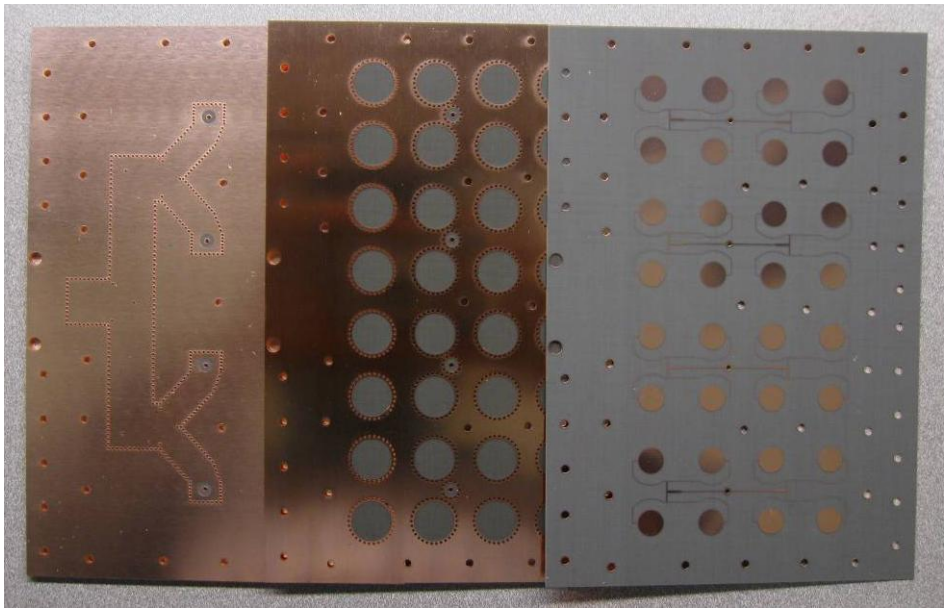


(b)

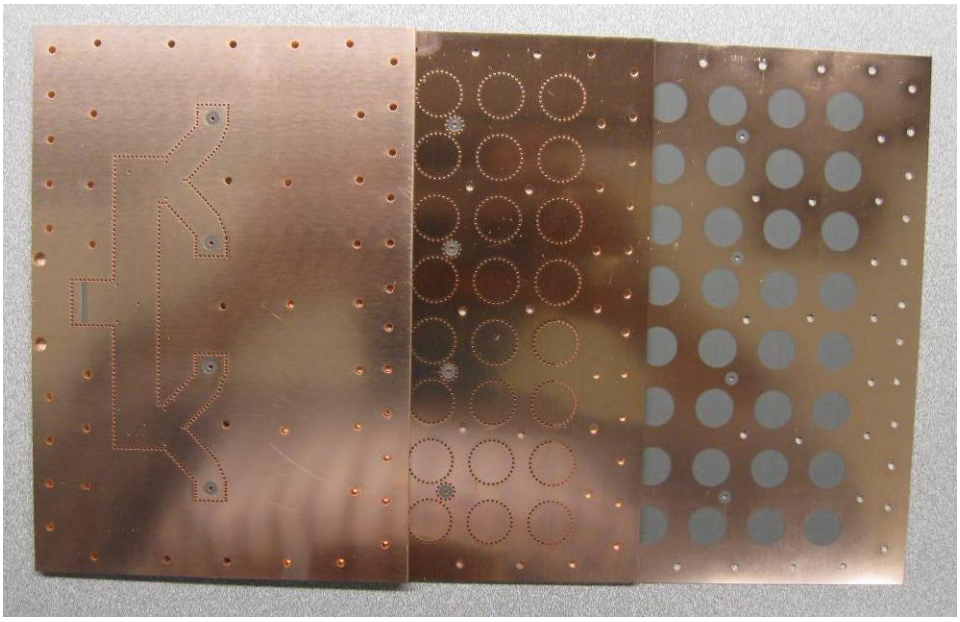
Figure 4.22 SIW one-to-four divider. (a) HFSS model. (b) Electric field distribution on the bottom surface.

4.5.3 **Experimental Results**

The SIW-fed 4x8 array has been fabricated, as shown in Figure **4.23** depicting the top and bottom views of the different constituting layers. Again Taconic TLY-5 has been utilized here for the three substrates with the same thicknesses used before in the 4x4 array.



(a)



(b)

Figure 4.23 Picture of the fabricated 4x8 SIW-fed array. (a) Top view. (b) Bottom view.

The fabricated array has been tested using an Agilent E86386 network analyzer to inspect its return loss performance. Figure **4.24** shows the measured reflection coefficient of the SIW-fed 4x8 array. The array exhibits a fractional bandwidth of 5% covering the required DBS band.

The far-field antenna normalized gain patterns of the 4x8 array measured at 12.5 GHz, are shown in Figure **4.25**, for the E- and H-plane cuts. The measured side lobe level is about -12 dB, while the cross-pol is better than -25 dB.

The measured gain versus frequency is shown in Figure **4.26** for the fabricated SIW-fed 4x8 array compared to that of the SIW-fed 4x4 array. Better than 2.4 dB increase in the gain is observed between the two different sized arrays along the DBS band of interest.

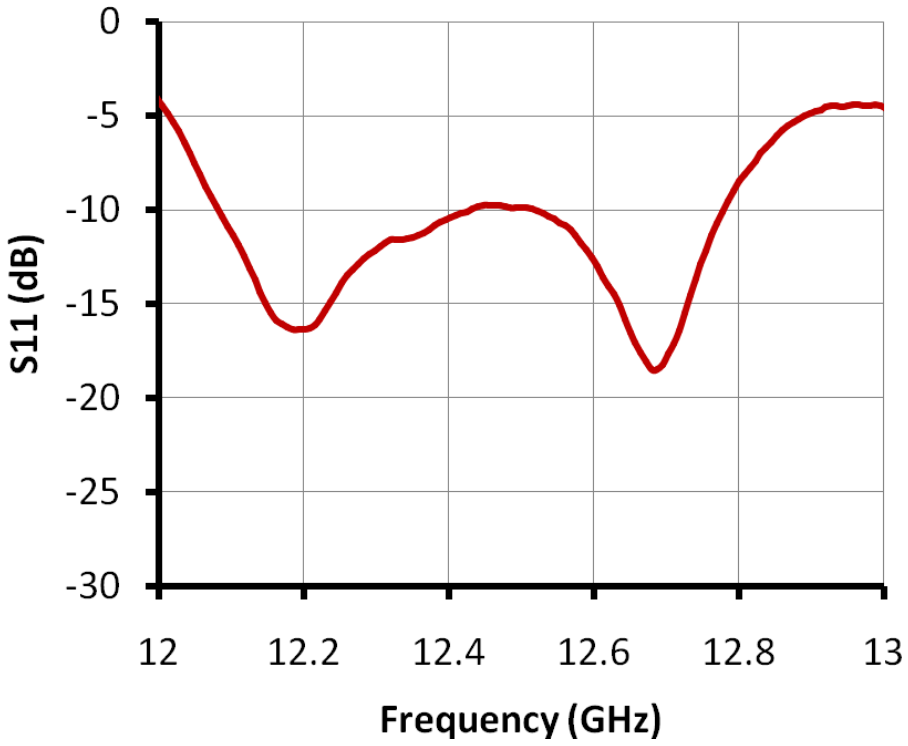
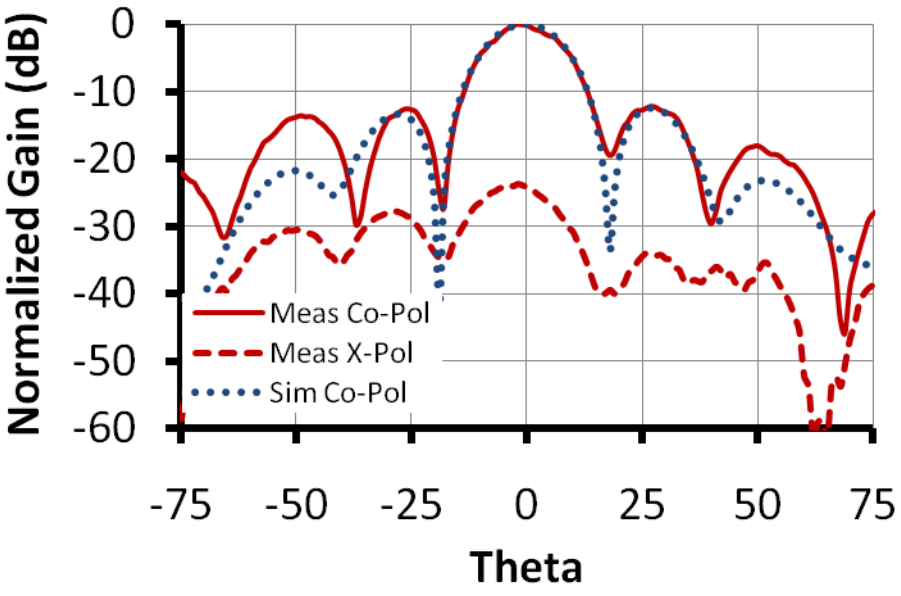
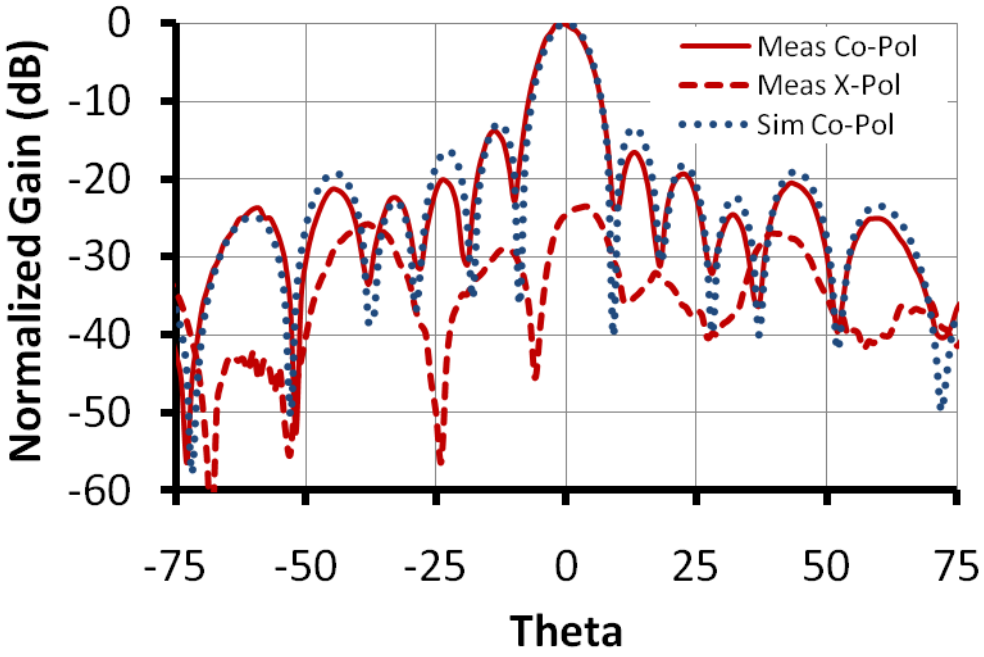


Figure 4.24 Measured reflection response of the 4x8 SIW-fed array.



(a)



(b)

Figure 4.25 Measured gain pattern of the 4x8 SIW-fed array at 12.5 GHz. (a) E-Plane. (b) H-Plane.

Again based on the single element gain of 8.6 dBi (at 12.5 GHz), we ideally expect about 23.6 dBi (at 12.5 GHz) gain for the array of 4x8 elements. However, the measured actual gain is 22.4 dBi (at 12.5 GHz). That leads us to estimate a 1.2 dB loss due to the feed network. Table **4.2** summarizes the losses of the different components that we have utilized in the feed network leaving 0.3 dB of unaccounted for losses that could be attributed to the assemblage of the structure.

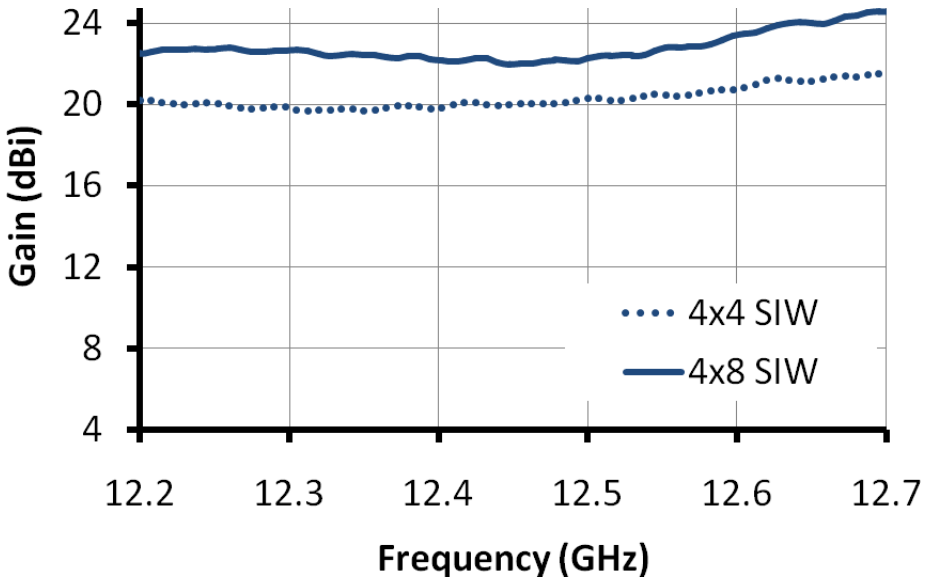


Figure 4.26 Measured gain vs frequency of the 4x8 SIW-fed array.

Table 4.2 Summary of losses in the various feed components of the SIW-fed 4x8 array

Component	Loss (dB)
Microstrip Feed Loss (2x4)	0.3
Microstrip to Coaxial Transition to SIW	0.2
SIW Feed	0.4
Unaccounted Losses	0.3

4.6 4x16 Array

4.6.1 **Array Configuration**

Finally, the SIW-feed topology has been used with larger array of 4x16 elements, as shown in Figure **4.27**. Again the array consists of three substrates; microstrip substrate, cavity substrate and feed substrate, however we used here the CPW feed transition shown before in Figure **4.7**. Unfortunately, we were not able to run an EM simulation for this large size array due to the need for exhaustive memory and long simulation time, so we will directly present our experimental results.

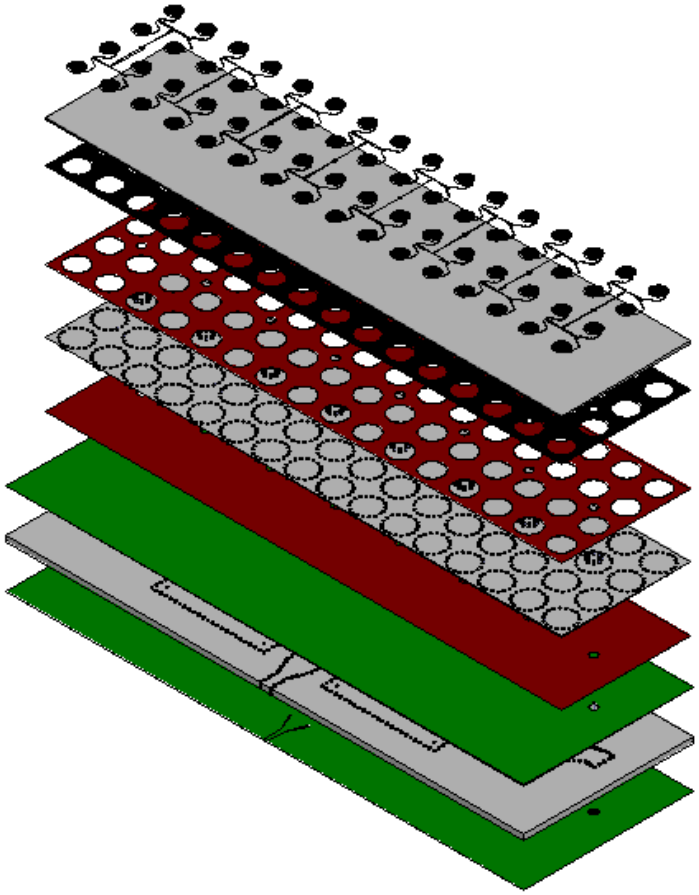


Figure 4.27 Array configuration of the 4x16 SIW-fed array depicting the different layers.

4.6.2 **Experimental Results**

The SIW-fed 4x16 array has been fabricated, as shown in Figure **4.28**, depicting the top view of the array. Rogers 5880 substrates of dielectric constant 2.2, loss tangent 0.0009, and of thicknesses 3.175 mm, 1.575 mm, and 0.381 mm has been utilized here for the feed, cavity and microstrip substrates, respectively.

The fabricated array has been tested using an Agilent E86386 network analyzer to inspect the return loss performance. Figure **4.29** shows the measured reflection coefficient of the SIW-fed 4x16 array which revealed a pump in the response around 12.3 GHz. This would relatively degrade the gain at the lower DBS band. A matching circuit could be used to resolve this problem.

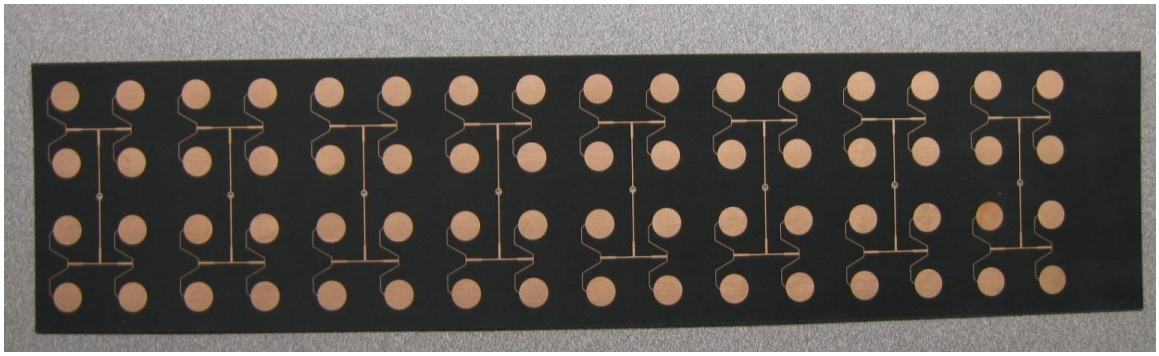


Figure 4.28 Picture of the fabricated 4x16 SIW-fed array.

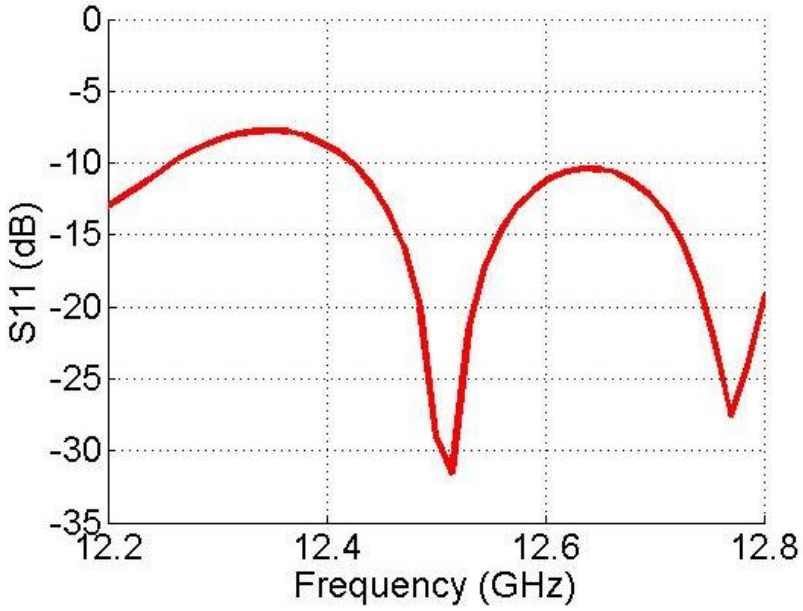
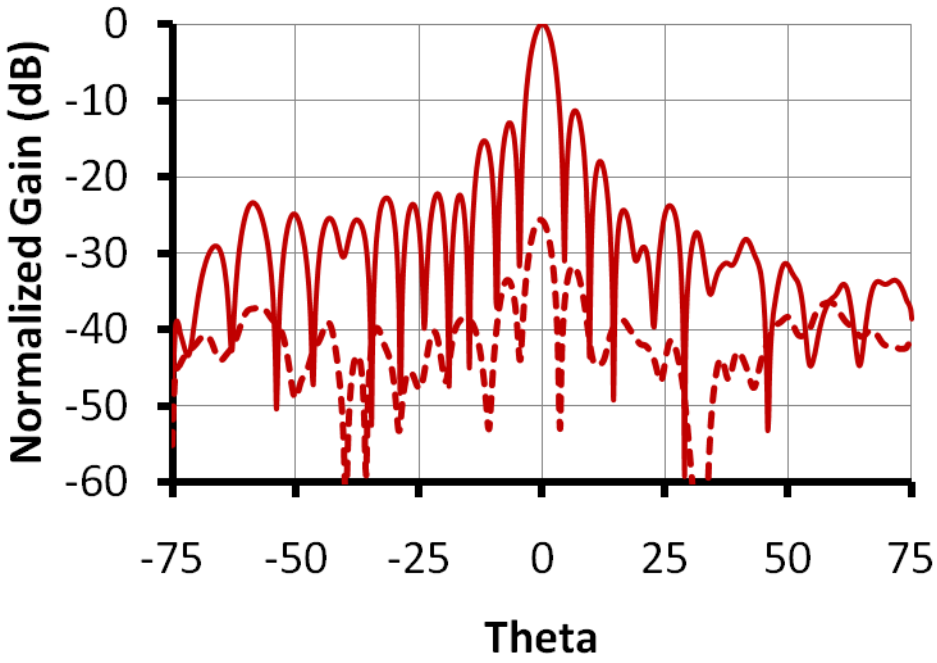


Figure 4.29 Measured reflection response of the 4x16 SIW-fed array.

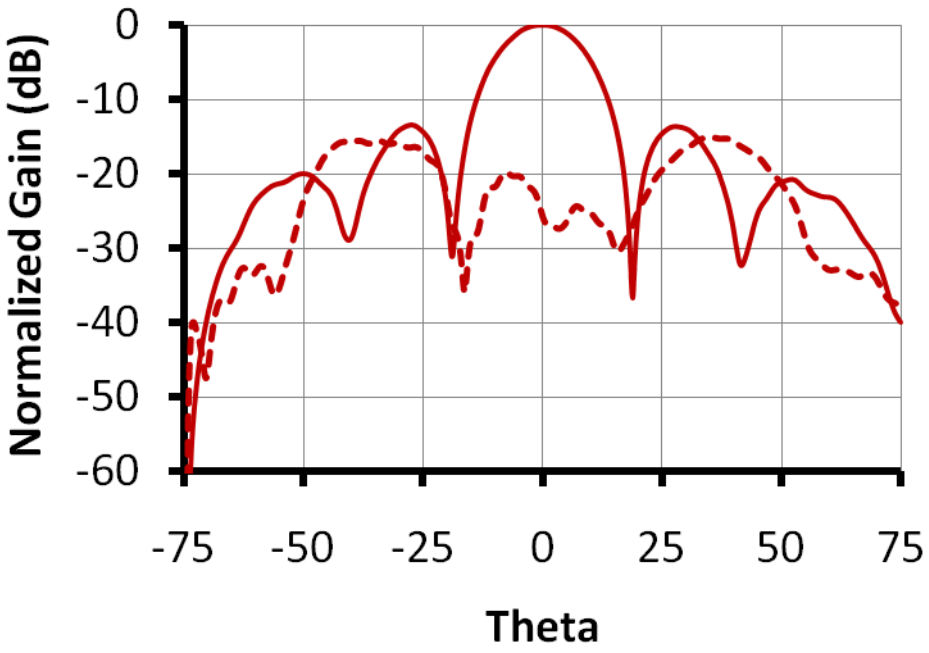
The far-field antenna normalized gain patterns of the array measured at 12.2 GHz, 12.45 GHz, and 12.7 GHz are shown in Figure **4.30**-32 for the E- and H-plane cuts. Measurements here have been done using a near field test facility at Winegard Company. The measured side lobe level is better than -12 dB, while the cross-pol is better than -20 dB at broadside at the three different frequencies.

Table **4.3** summarizes the performance of the 4x16 array in terms of gain, side-lobe level and cross-pol at the three different frequencies. The gain at a 12.45 GHz is 24.3 dBi which is better than that demonstrated before for the microstrip 8x8 array in Chapter3 (24 dBi) by 0.3 dB. The gain of the array could be even improved by using a better waveguide feed transition instead of the CPW one. However, there is a gain drop at 12.2 GHz, and relatively poor match around. Based on measurements, the gain drop at the lower end could be related to some structure internal resonance, as seen by almost 7 dB return loss at 12.3 GHz.

Again based on the single element gain of 8.6 dBi (at 12.45 GHz), we ideally expect about 26.6 dBi (at 12.45 GHz) gain for the array of 4x16 elements. However, the measured actual gain at the same frequency is 24.3 dBi. That leads to our estimate of 2.3 dB loss due to the feed network. Table **4.4** shows our estimate of the losses of the different components we have utilized in the divider leaving 0.5 dB of unaccounted losses that could be attributed to the assemblage of the structure. It is clear that the 2.3 dB drop is significant, better assembly could help in retrieving back a 0.5 dB, but still more than 1 dB is due to the SIW feed network and its transition and would require extensive redesign or use of thicker feed substrate.

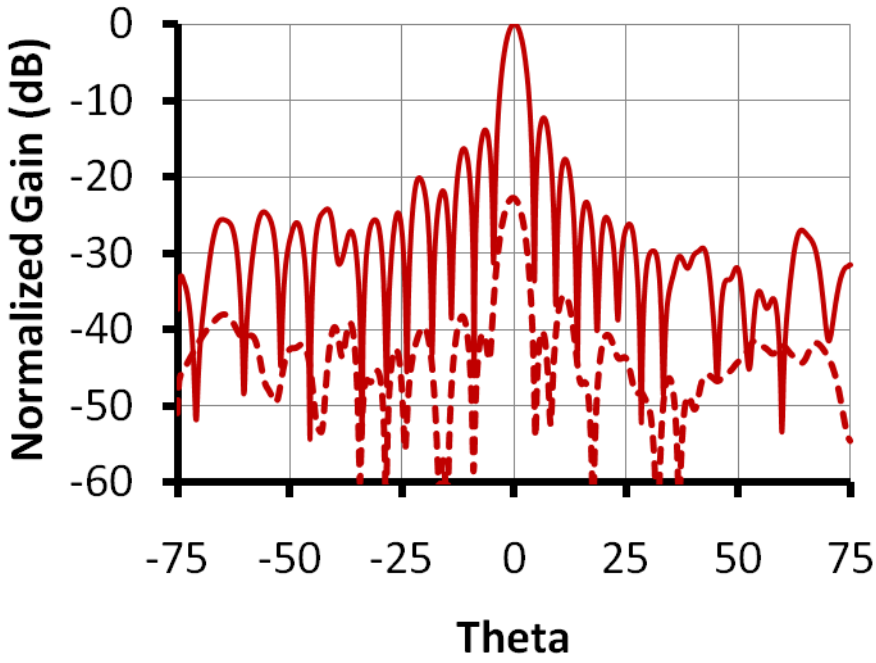


(a)

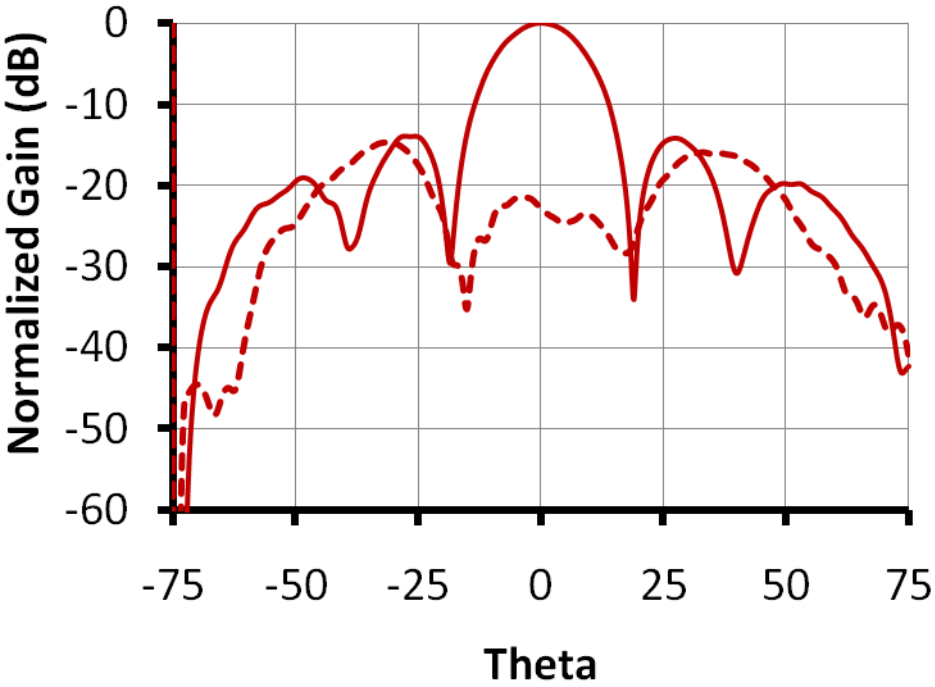


(b)

Figure 4.30 Measured gain pattern of the 4x16 SIW-fed array at 12.2 GHz. (a) E-Plane. (b) H-Plane.

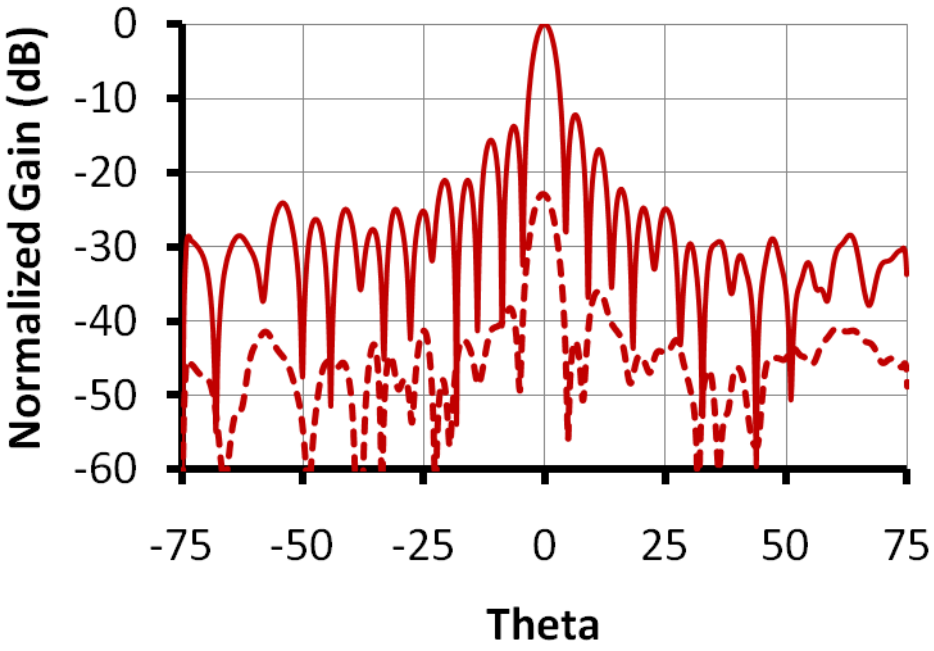


(a)

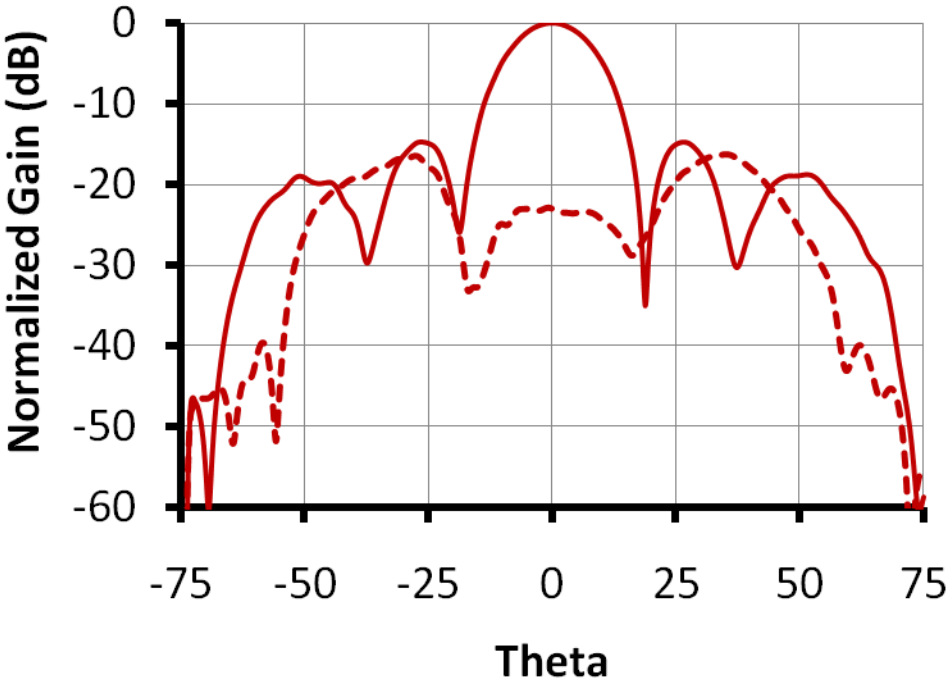


(b)

Figure 4.31 Measured gain pattern of the 4x16 SIW-fed array at 12.45 GHz. (a) E-Plane. (b) H-Plane.



(a)



(b)

Figure 4.32 Measured gain pattern of the 4x16 SIW-fed array at 12.7 GHz. (a) E-Plane. (b) H-Plane.

Table 4.3 Summary of the performance of the 4x16 array

Frequency	Gain(dBi)	Sidelobe level (dB)	Cross Pol level (dB)
12.20 GHz	23.64	-12.0	-25.59
12.45 GHz	24.31	-12.5	-22.73
12.70 GHz	24.49	-12.5	-22.94

Table 4.4 Summary of losses in the various feed components of the SIW-fed 4x16 array

Component	Loss (dB)
Microstrip Feed Loss (2x4)	0.3
Microstrip to Coaxial Transition to SIW	0.2
SIW Feed	0.7
CPW Transition Feed	0.4
SMA Input Connector	0.2
Unaccounted Losses	0.5

4.7 Conclusion

The substrate-integrated waveguide feed offers the potential to lower the relatively higher losses associated with the long microstrip feed lines, yet at much lower cost when compared to the conventional waveguide feed topologies. Teaming up the SIW feed with the SIW cavities secures a potential antenna solution with relatively good bandwidth controlled by the cavity height and also good efficiency sustained by the SIW feed. The proposed array structure can be a good candidature for DBS applications if a solution could be found for the dual polarization issue, which will be addressed in next chapter.

At this time, only slight improvement in gain has been demonstrated in comparison to the microstrip fed array for the large 4x16 array. It is believed that use of a better method for assembly different than using screws to hold the three layers, and further improvement of the SIW feed like using thicker feed substrate layer could improve the performance and makes it more attractive.

Chapter 5 Dual-Polarized Low-Profile SIW Cavity-Backed Patch Array for DBS Applications

In this chapter, we extend the SIW-fed cavity-backed patch arrays to provide dual polarization. First, we will design a small dual-polarized array of 2x4 elements cluster sub-array, then will be extended to develop a larger array of 4x16 elements which is comprised of eight of these clusters-sub-arrays. In both cases an extra column was added to simplify the feed of two polarizations, i.e. 3x4 and 4x17 elements will be used instead. Similar to the previously developed single polarized SIW-fed array, microstrip feed networks are utilized to feed the sub-arrays, while coaxial probes are interconnecting the SIW low loss feeds and the microstrip dividers. Two separate feed networks are used, one for each polarization.

5.1 Introduction

Previously, several designs have been proposed to develop a dual-polarization capability for DBS antennas. One of the early designs is the radial line slotted array, shown in Figure **5.1**, developed by Takahashi et. al . in [78] (after a lot of work on the radial line slotted arrays by the group of Professor. Ando in Japan [79-90]). Despite the capability of the radial line slotted array antenna in simultaneously receiving the LHCP and RHCP, the antenna renders thick profile as it has broadside beam and need to be tilted over a scan volume of 20- 70º to fully track the satellite. Moreover, the structure also is relatively complicated in fabrication and assemblage.

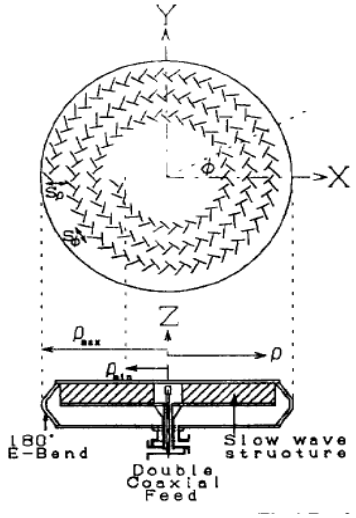


Figure 5.1 Dual-polarized radial line slotted array developed by Takahashi et. al. [77].

Another DBS antenna structure developed for simultaneous dual polarization operation have been developed by Prof. Safavi-Naeini's group at Waterloo University [91], as shown in Figure **5.2** (several trials have been conducted before reaching this design [18, 35, 92]). They developed a split aperture low-profile patch array by dividing the antenna area into several low height boards; each board is 40 mm in width. Authors have separated, however, the two circular polarizations in distinct cascaded boards that would significantly lower the overall aperture efficiency of the antenna, but would simplify the feed structure.

As we mentioned before in our introduction in Chapter 1, S. Yang [37] developed also a slotted array antenna for DBS. His antenna is a low profile substrate integrated waveguide (SIW) array, made of 32 waveguides with 13 cross slots each, and is shown again in Figure **5.3**. The inherent tilted beam of the leaky wave antenna considerably reduced the mechanical steering requirements. Unfortunately, such an antenna could receive only one circularly polarized signal at a time; either LHCP or RHCP one.

Park, et. al. in [93] presented a mobile antenna for multimedia communications with Ku-band geostationary satellite KOREASAT-3 and JSAT-2A. The proposed mobile antenna provided dual circular polarization by utilizing dual-corner fed microstrip patches, as shown in Figure **5.4**. They have utilized also phased array for electronic scanning.

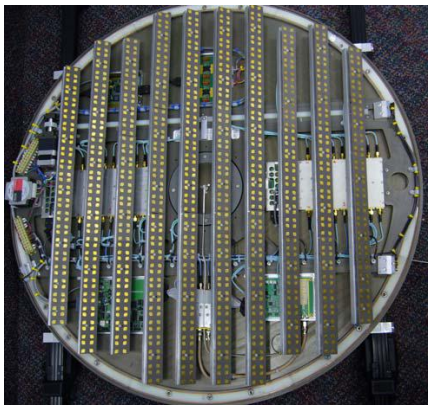


Figure 5.2 Dual-polarized DBS antenna developed by the group of Prof. Safavi-Naeini [91].

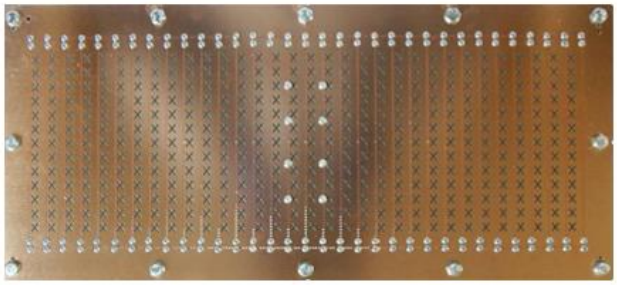
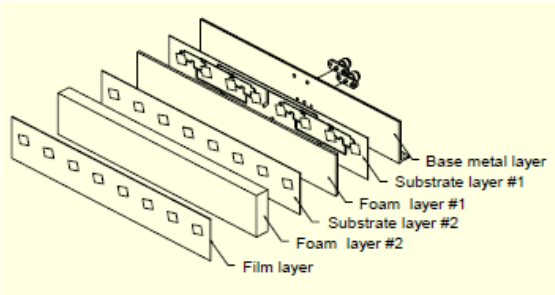


Figure 5.3 Cross-slotted substrate-integrated waveguide antenna proposed by S. Yang [37].



(a) (b)

Figure 5.4 DBS antenna array proposed by Park et. al [79].

Table **5.1** summarizes the performance of the previously developed dual-polarized DBS arrays.

Table 5.1 Comparison between the previously developed dual-polarized DBS antennas

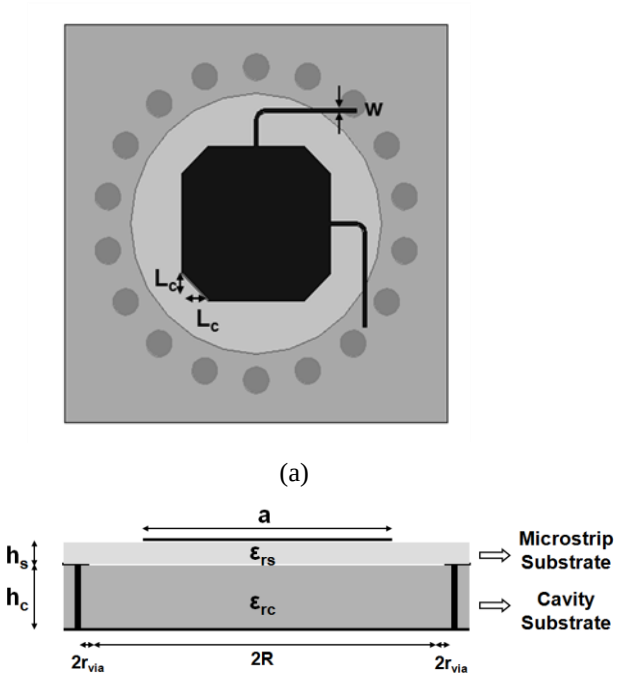
	Takahashi et. al.	**Mousavi et. al.**	**Yang et. al.**	**Park et. al.**
Radiating Structure	Slotted Radial Line	Suspended Microstrip Patch	Slotted Waveguide Array	Microstrip Patch
Beam Direction	Broadside	Broadside	45° Tilted	Broadside
Polarization	LHCP/RHCP	LHCP/RHCP	LHCP or RHCP	LHCP/RHCP
Gain	33.4 dBi/32.7 dBi (12.5 GHz/12.55 GHz)	31.5 dBi	26.52/26.17 dBi (12.45 GHz)	N/A
Steering	Mechanical	Electronic	Mechanical	Electronic

In the following we will describe first the single element design, followed by the details of the sub-array, and then briefly discuss the waveguide feed network. Finally, we will demonstrate the full dual-polarized array performance.

5.2 Single Element Design with Dual Feed

It has been lots of research on using a single patch with two orthogonal feed lines to provide dual polarization radiation with adequate isolation [2]. Figure **5.5** shows our dual-fed patch element implementation, where two orthogonal narrow-width microstrip lines are feeding the patch element. In this implementation, the single element is designed using two substrates; a microstrip substrate and a cavity substrate like the previously developed single polarization patch in Chapter 3. Here, we use trimmed square patches for our initial single and sub-array designs, but for the large array we will switch to circular patches to achieve slightly higher gain.

The design guidelines previously developed in Chapter 3 for the single-fed patch were utilized here too with the dual-polarized patch, however fine optimization generally might be required to extend single feed design to dual feed design. Same dimensions were used for the dual polarized case as shown in Figure **5.6**, where adequate isolation between the two feeds was sustained. The single element performance was simulated using HFSS and it exhibited an acceptable matching performance (> 12 dB return loss) for the two polarizations over the required DBS band of interest, and the simulated isolation is better than 18 dB. It is interesting to recognize that it is difficult to align the match of the two feeds of the two orthogonal polarizations to the same central frequency, as seen in Figure **5.6**.



(a)

(b)

Figure 5.5 Dual-polarized SIW cavity-backed microstrip patch single-element (a) Top view. (b) Side view.

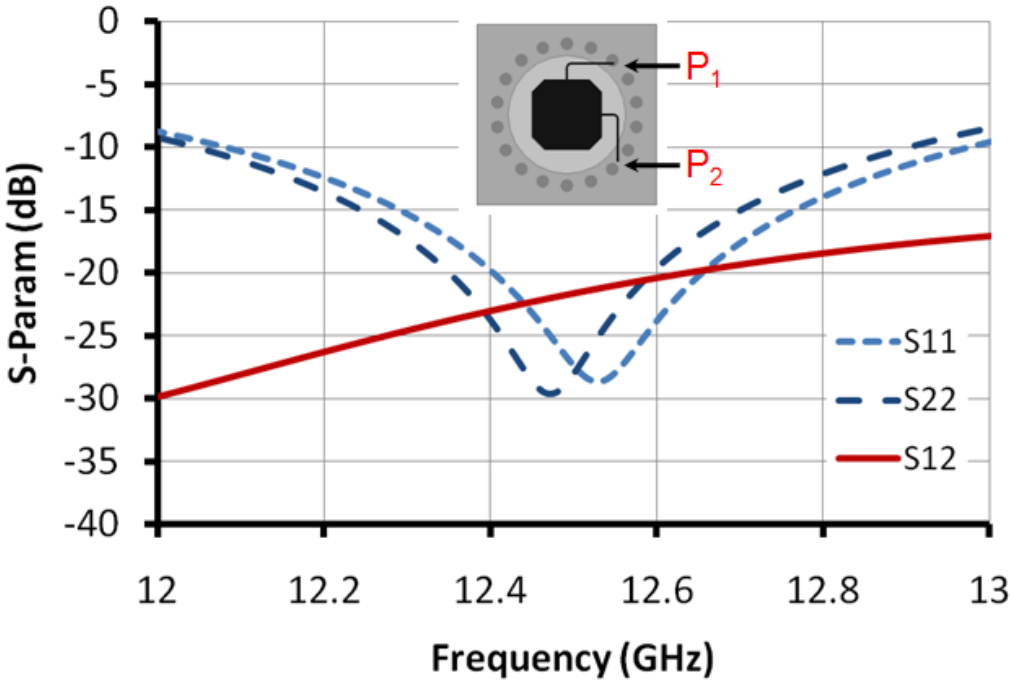


Figure 5.6 Simulated reflection coefficient of the proposed dual-polarized single element (for ε_{rs}=2.2, h_s=0.381 mm, ε_{rc}=2.2, h_c=1.575 mm, a=7.2, R=0.84a, L_c=a/5, w=0.15 mm, r_{via}=0.635mm).

5.3 Sub-Array Configuration

Based on the single element design discussed in the previous section a 3x4 dual polarized sub-array was developed. The dual polarized sub-array basically consists again of a stack of two substrates namely; microstrip substrate of dielectric constant ε_{rs} and a cavity substrate of dielectric constant ε_{rc}, as shown in Figure 5.7(b). Trimmed square patches of side length *a* were printed on the microstrip substrate, while being fed through a staggered dual probe-fed microstrip dividers; one provides the horizontal polarization (1st divider), while the second provides the vertical polarization (2nd divider), as shown in Figure 5.7(a). As seen from Figure 5.7, the array has effectively 2x4 elements for each polarization. The grounds of the microstrip substrate and the top layer of the cavity substrate have circular openings of radius *R* underneath the patches. Many via holes spaced along the circular openings were drilled in the cavity substrate and were through platted constituting the SIW circular cavities backing the patches, as shown in Figure 5.7.

An integrated 50Ω coaxial probe feed topology is again adopted to excite the antenna sub-array, as shown in Figure 5.7(a). It is worth noting that rather than feeding each two patches symmetrically from the similar sides, the patches of each 2x2 sub-array are fed from opposite sides to simplify staggering both the vertical and horizontal feed networks in the available space. Opposite feeding causes the feeding

currents to be out-of-phase, then a 180º differential phase shift at the center frequency is utilized in both networks to compensate for that opposite feed topology.

Meanwhile, the design of the dual-polarized 3x4 sub-array is essentially based on the performance of the corresponding single-polarized 2x4 sub-arrays, shown in Figure **5.8**. In that perspective, we will first demonstrate the performance of the single polarized sub-arrays, both the horizontally and vertically-polarized ones. Then cascading those two sub-arrays in one structure constitutes the combined 3x4 sub-array.

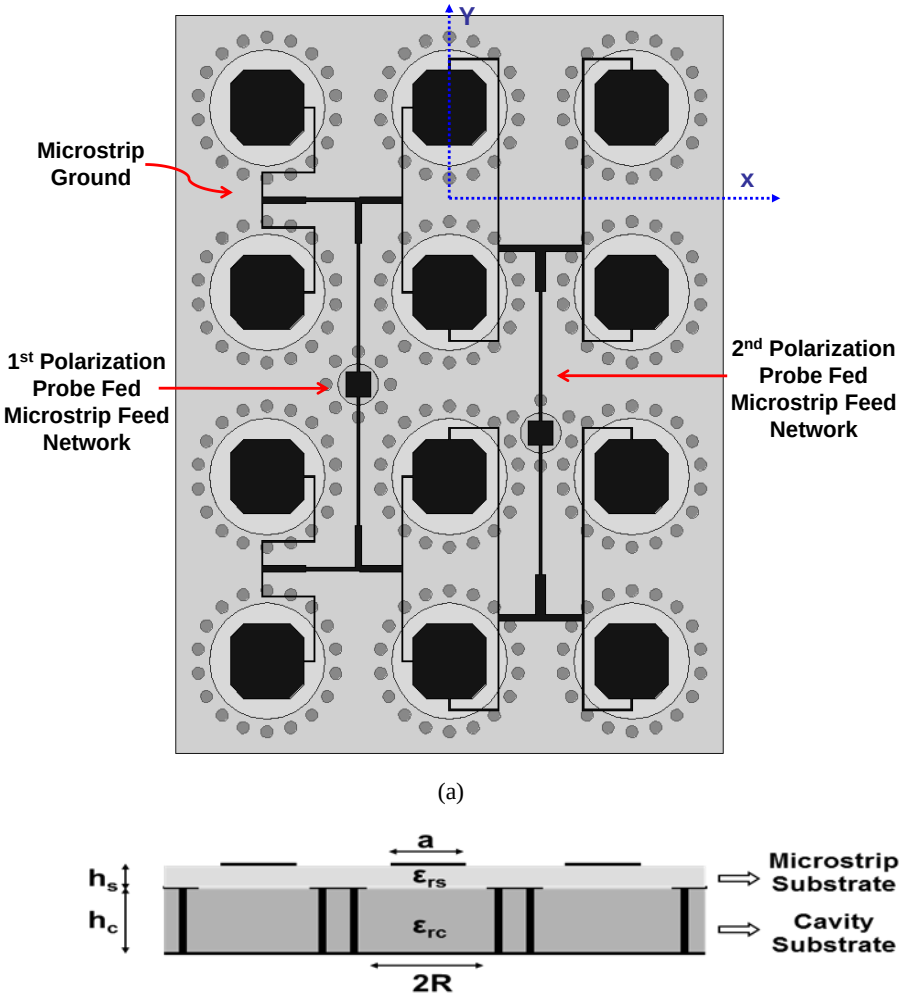


Figure 5.7 Proposed substrate-integrated cavity-backed microstrip patch 3x4 subarray with dual linear/circular polarization.

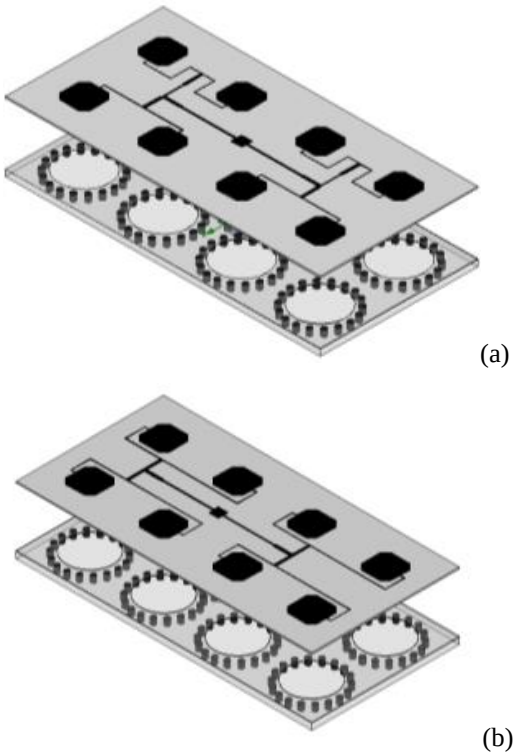


Figure 5.8 Single polarized corresponding 2x4 sub-arrays (layers are spaced apart to show the SIW cavities), (a) Horizontally-polarized. (b) Vertically-polarized.

To that end, the design of the SIW cavity-backed patch antenna involves as usual the selection of the substrate properties (thickness and dielectric constant) and the determination of the patch and cavity dimensions. Following the design guidelines presented in Chapter 3, we have used a 0.381 mm thin Rogers 5880, a quite thin substrate ~ 0.02 λ_0, for the microstrip feed and patch printing to minimize the feed network losses. Then for the cavity substrate, we have used the same material, Rogers 5880, however of 1.575 mm ~ 0.066 λ_0 in thickness to achieve better than 5% fractional bandwidth.

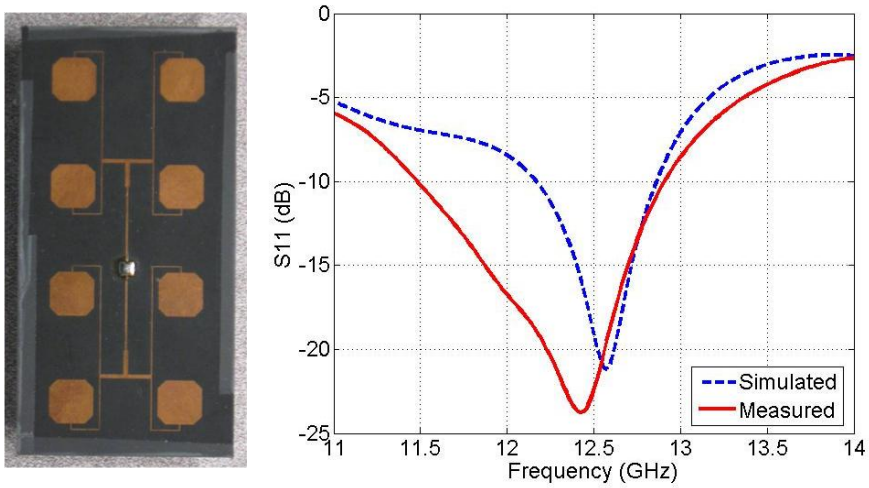
5.3.1 **Experimental Results**

The proposed dual-polarized sub-array along with its single polarized constituents have been fabricated. Standard SMA with a solder cup contact was utilized in exciting the antenna structure. The performance of the single polarized 2x4 sub-arrays will be first demonstrated in the following section.

5.3.1.1 2x4 Vertically Polarized Sub-Array

Picture of the fabricated 2x4 vertically polarized sub-array is depicted in Figure **5.9**(a). Figure **5.9**(b) shows the return loss of the sub-array, that was measured using Agilent E86386 network analyzer, versus the numerically simulated one. The measured and the simulated responses are in good agreement except

of a slight frequency shift of less than 1%. On the other hand, the far field measured antenna gain pattern at 12.5 GHz is shown in Figure **5.10** for YZ cut. The side lobe level is about -14 dB, while the cross-pol is about -20 dB lower than broadside, as shown in Figure **5.10**. The 2x4 sub-array exhibits a gain of about 16.5 dBi (compared to 16.7 dBi simulated value) at 12.5 GHz, while the aperture radiation efficiency is better than 70% over the DBS frequency range.



(a) (b)

Figure 5.9 Vertically-polarized 2x4 sub-array. (a) Picture of the fabricated structure. (b) Measured vs. simulated return loss.

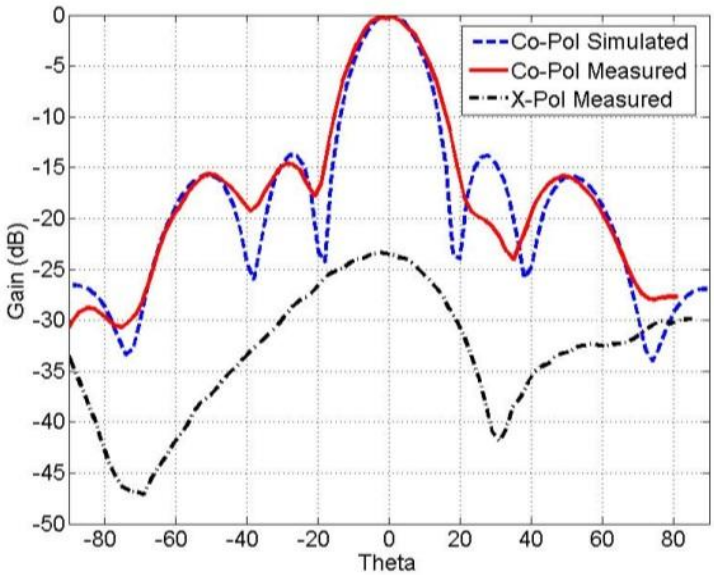
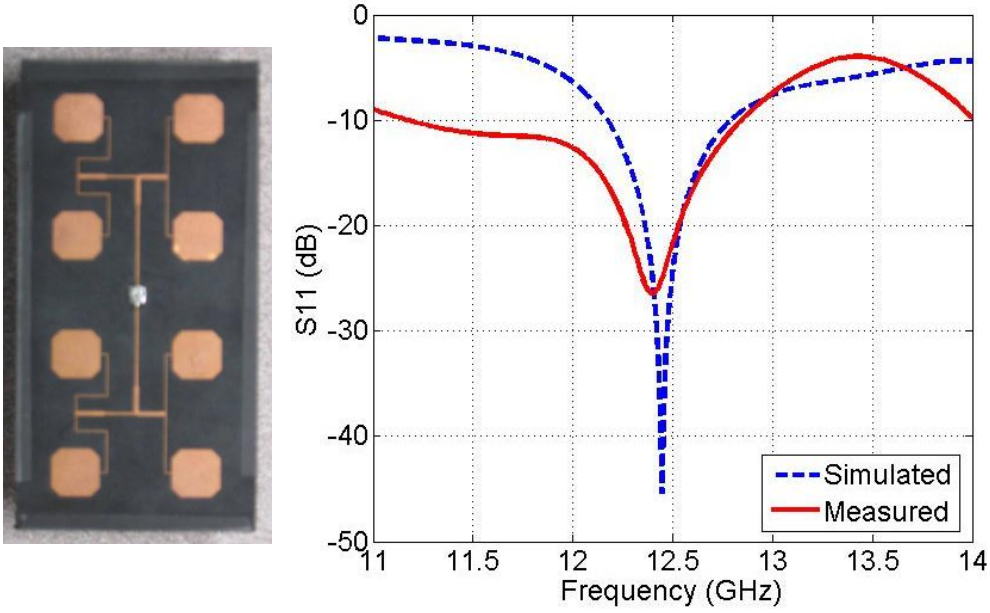


Figure 5.10 Measured vs. simulated radiation pattern at 12.5 GHz of the vertically-polarized 2x4 sub-array for the YZ-cut.

5.3.1.2 2x4 Horizontally Polarized Sub-Array

Similarly, the horizontally-polarized sub-array was fabricated, as shown in Figure **5.11**(a), and experimentally tested, as shown in Figure **5.11**(b), for the return loss performance, and in Figure **5.12** for the radiation pattern. The measured return loss is a bit wider than the simulated one, while there is again a slight frequency shift, as shown in Figure **5.11**(b). On the other hand, the side lobe level is slightly degraded in this structure to about -11.5 dB down, while the cross-pol is lower than -20 dB, as shown in Figure **5.12** (i.e. very similar to the measured value of the vertically polarized sub-array). The 2x4 sub-array exhibits a gain of about 16.6 dBi (compared to 16.7 dBi simulated value) at 12.5 GHz, while the aperture radiation efficiency is again better than 70% over the DBS frequency range. These results are very similar to that of the 2x4 microstrip array demonstrated previously in Chapter 3 without the opposite feed; which is very encouraging.



(a) (b)

Figure 5.11 Horizontally-polarized 2x4 sub-array. (a) Picture of the fabricated structure. (b) Measured vs. simulated return loss.

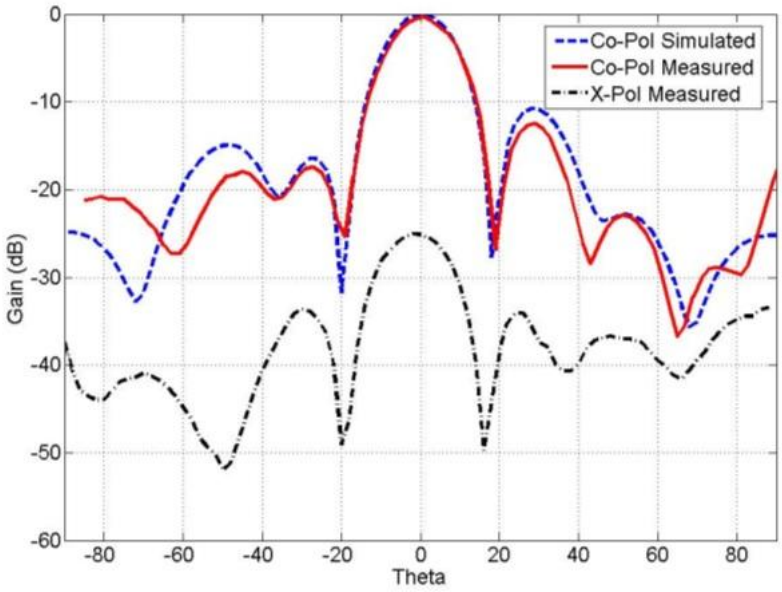
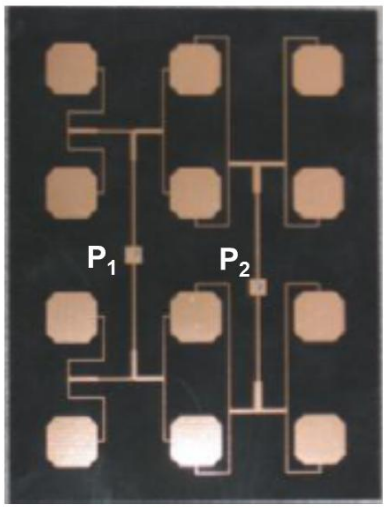


Figure 5.12 Measured vs. simulated radiation pattern at 12.5 GHz of the horizontally-polarized 2x4 sub-array for the YZ-cut.

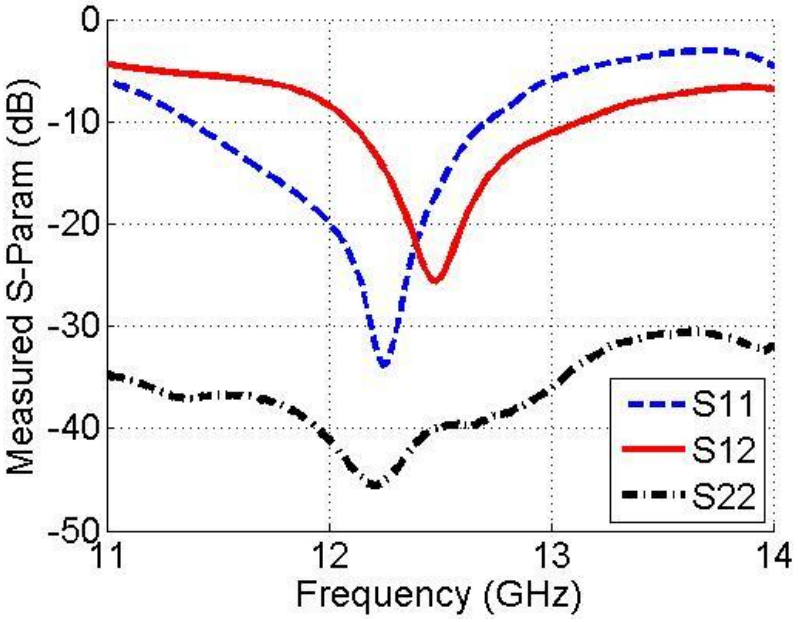
5.3.1.3 3x4 Dual- Polarized Sub-Array

Finally, a dual-polarized sub-array is attained upon combining the 2x4 single-polarized structures demonstrated before and building 3x4 instead. The sub-array was fabricated as shown in Figure **5.13**(a). The measured reflection coefficient response of the two ports is shown in Figure **5.13** (b). The sub-array covers the required DBS frequency range (12.2-12.7 GHz) at both ports while the isolation between the two ports is better than -35 dB along the band of operation.

Measurements of the far field antenna radiation patterns at 12.5 GHz of both polarizations are shown in Figure **5.14** for the YZ cut. The side lobe level is better than -14 dB, while the cross-pol is better than -19 dB (at broadside) in both cases, as shown in Figure **5.14** (a), and (b) for the horizontal, and vertical polarization excitations, respectively.

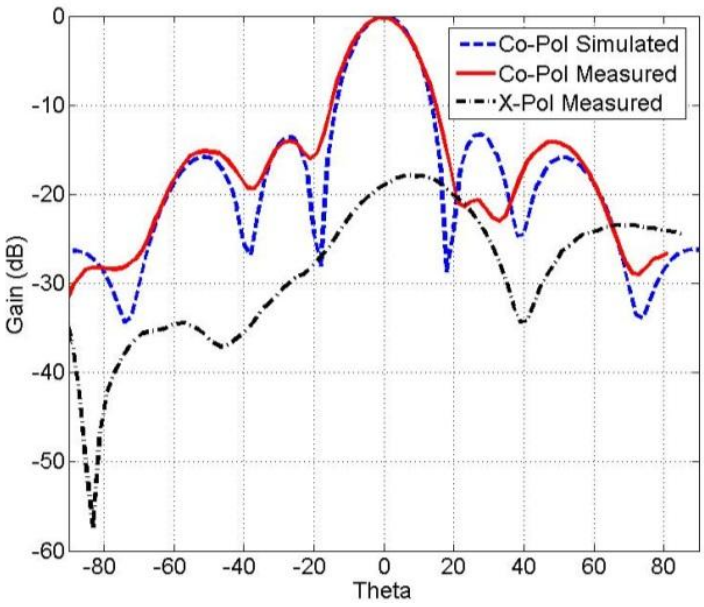


(a)

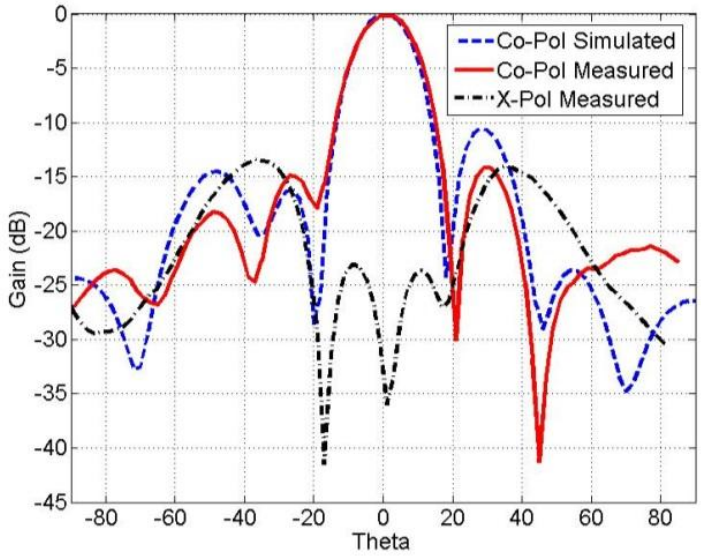


(b)

Figure 5.13 Dual linearly-polarized 3x4 sub-array. (a) Picture of the fabricated structure. (b) Measured S-parameters showing the reflection response of the two feeding ports and the mutual coupling between them (P_1 is the excitation of horizontal polarization while P_2 is the vertical one).



(a)



(b)

Figure 5.14 Measured radiation pattern (solid) vs. the simulated one (dotted) of the cavity backed microstrip patch 3x4 sub-array. (a) YZ-cut while $port_1$ (horizontal) is excited and $port_2$ (vertical) is matched. (b) YZ-cut while $port_2$ (vertical) is excited and $port_1$ (horizontal) is matched.

The measured gain vs. frequency is shown in Figure **5.15**. The sub-array exhibits a gain at 12.5 GHz of about 16.2 dBi and 16.5 dBi for the horizontal and vertical polarization, respectively; which is a slightly lower than the single polarized corresponding sub-arrays, especially for the horizontally-polarized one. However, over the 12.2 to 12.7 frequency range a 0.8-1.2 dB gain degradation was seen and most probably is attributed to the relatively higher mutual coupling effects existing in the 3x4 sub-array and the sub-array needs to be further optimized to reduce this effect.

Table **5.2** compares the measured gain performance of the dual versus single polarized sub-arrays.

Despite that the demonstrated sub-array is being fed through staggered dual linear excitations, combining the two excitations using a quadrature hybrid should provide dual circular polarization, as well.

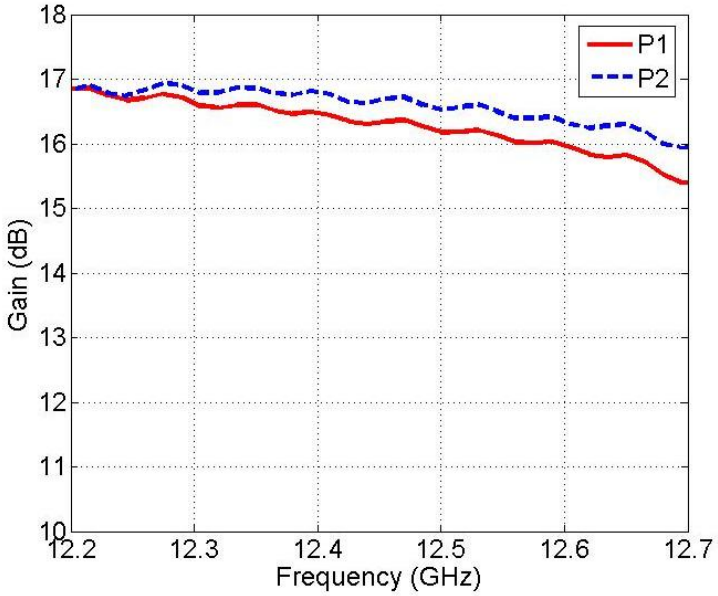


Figure 5.15 Measured gain versus frequency for both polarization ports (P_1 is the excitation of horizontal polarization while P_2 is the vertical one).

Table 5.2 Summary of the measured gain performance of the dual vs. single polarized sub-arrays

	Horizontal Pol Single Pol (dBi)	Horizontal Pol. Dual Pol (dBi)	Vertical Pol. Single Pol. (dBi)	Vertical Pol. Dual Pol.(dBi)
12.20 GHz	16.4	16.8	16.9	16.8
12.45 GHz	16.6	16.3	16.5	16.5
12.70 GHz	16.1	15.5	16.0	16.0

5.4 Feed Network

In order to attain a dual polarized large array we have adopted a binary feed network design that will be demonstrated in this section.

5.4.1 SIW Feed Design

Similar to [14] we have utilized a twin one-to-eight SIW binary feed network, shown in Figure **5.16**, as a feed to a 4x17 array of the cavity-backed microstrip patches, shown in Figure **5.17**. The SIW divider is excited by coplanar flared transition (previously introduced in Chapter 4). Each branch of the divider ends by a via probe excitation that goes through a stack of three substrates; the feed substrate then the cavity substrate and finally the microstrip substrate delivering the electromagnetic wave to the microstrip line dividers. Rogers RT/duroid 5880 substrate with a relative dielectric constant 2.2, and of a thickness 3.175 mm was used for the feed substrate. The use of three layers and the fact that probes need to go through the three layers are relatively problematic from manufacturing point of view.

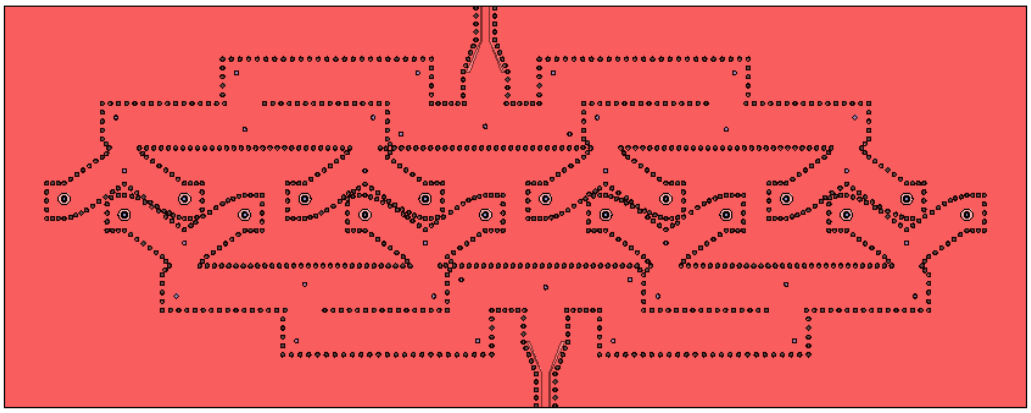


Figure 5.16 Twin one-to-eight SIW binary waveguide divider.

5.5 Full Dual-Polarized SIW-Fed Array

5.5.1 **Array Configuration**

Figure **5.17** shows the array configuration of the full dual-polarized SIW-fed array indicating the different consistuting layers. As mentioned earlier, circular patches have been used here instead of the trimmed square patches, previously utilized in the sub-array, to relatively increase the gain (Circular patches have better gain rather than the rectangular patches as demonstarted before in Chapter 2).

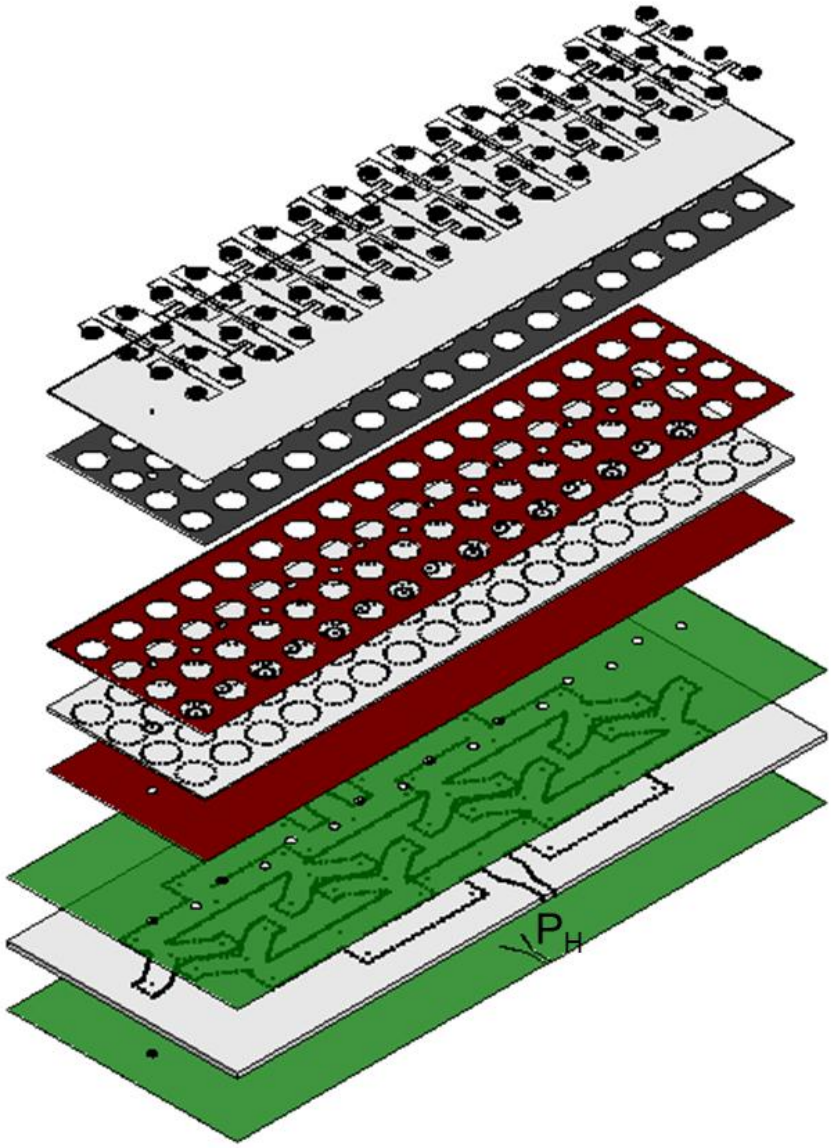


Figure 5.17 Proposed SIW cavity-backed microstrip patch full array (the CPW excitation of the horizontal polarization is shown in the bottom right while the vertical one is hidden but should be on the other side).

5.5.2 **Experimental Results**

The full 4x17 array has been fabricated as shown in Figure **5.18** . Rogers RT/duroid 5880 substrate with relative dielectric constant of 2.2 and thickness of 0.38 mm was utilized for the microstrip substrate while the same substrates, however with thickness of 1.58 mm, 3.175 mm were used for the cavity substrate and feed substrate, respectively.

5.5.3 **Reflection Response**

The fabricated array was tested using an Agilent E86386 network analyzer to inspect its return loss performance. Figure **5.19** shows the measured return loss of the dual-polarized array for both polarization ports. The vertical polarization port (S_{11}) exhibits relatively good matching performance over the DBS frequency band of interest, while the horizontal polarization port (S_{22}) is having unfortunately a matching problem at the lower band edge.

5.5.4 **Radiation Patterns**

The normalized far-field gain patterns of the array have been measured using near field set-up at Winegard company, as shown in Figure **5.20**-25, at both the band edge frequencies 12.2, 12.7 GHz and center frequency 12.45 GHz. The array exhibits better than -12 dB relative side-lobe level and -20 dB cross-pol level over the band.

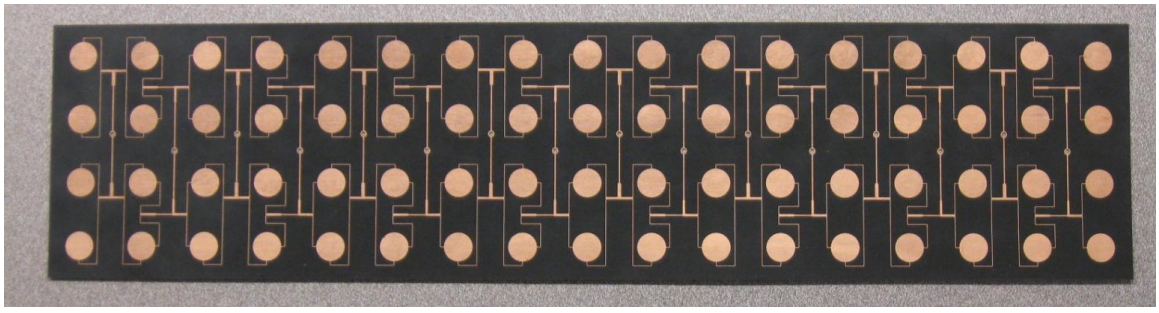


Figure 5.18 Picture of the fabricated dual-polarized array.

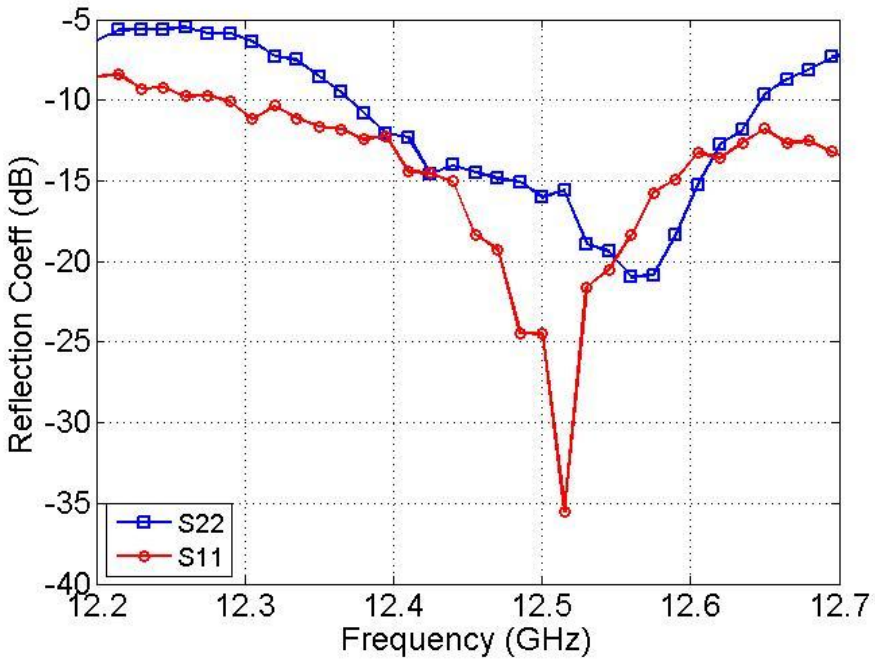
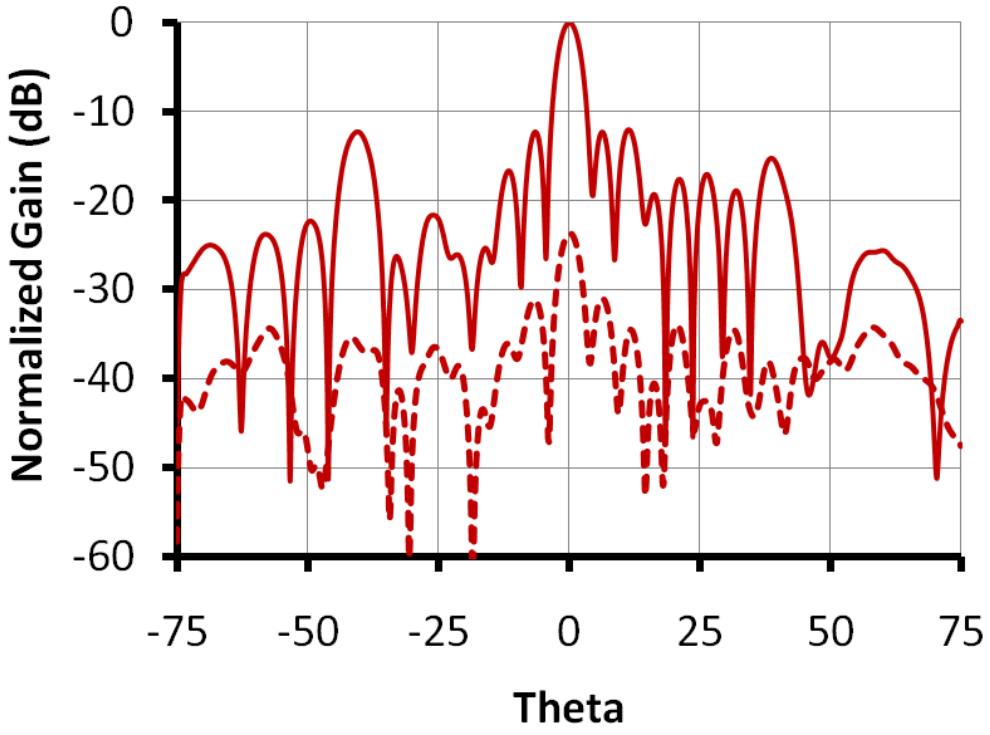


Figure 5.19 Measured reflection coefficients of the proposed dual-polarized array ($port_1$ is vertical, $port_2$ is horizontal)

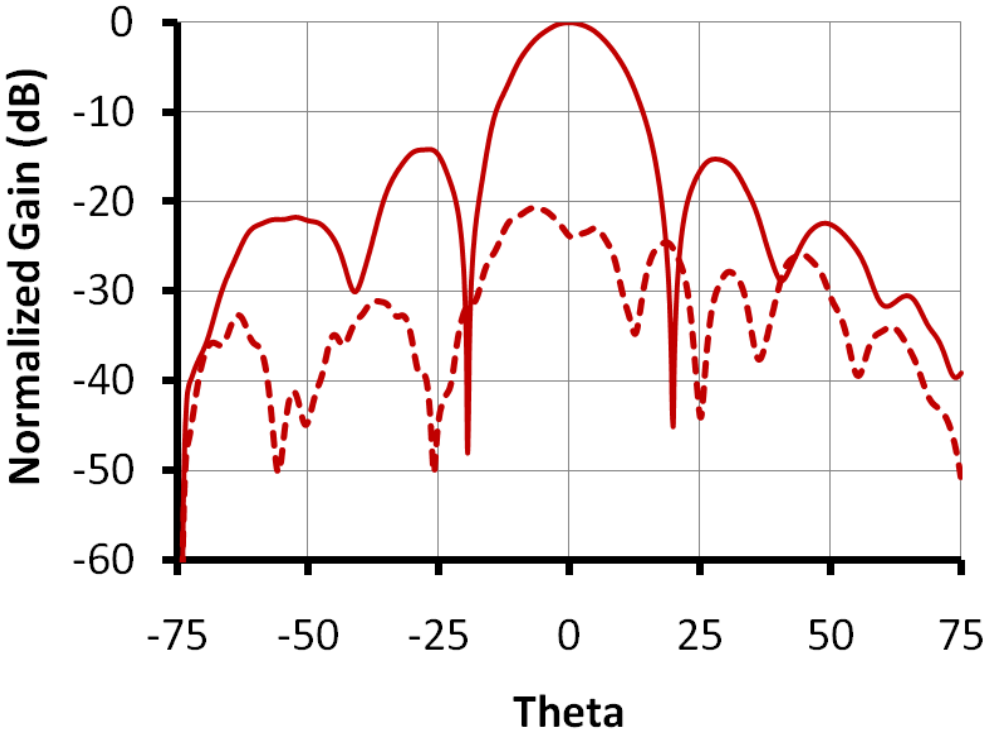
Table **5.3** summarizes the performance of the array as a function of frequency showing the gain, side-lobe level, and cross-pol level. As expected the horizontal polarization has relatively lower gain at the lower band edge because of the poor matching.

To see the effect of poor match on the gain performance, we re-calculated the gain after accounting for the loss due to poor input match as listed in Table **5.3**. Definitely, much uniform gain as function of frequency can be seen upon accounting for the match losses. At this point, it is not clear if it is a design problem or an assembly problem, simulation of the large array with the dual polarization was prohibitive due to the need for large memory.

Table **5.4** lists also the losses of the different components used in the feed network. The losses in the dual polarized array is a little higher than expected due to the assemblage and mutual coupling between the dual staggered feed. However, the overall aperture efficiency (about 53%) is still relatively good compared to [91], where separate cascaded panels were adopted to acquire the dual-polarization operation.

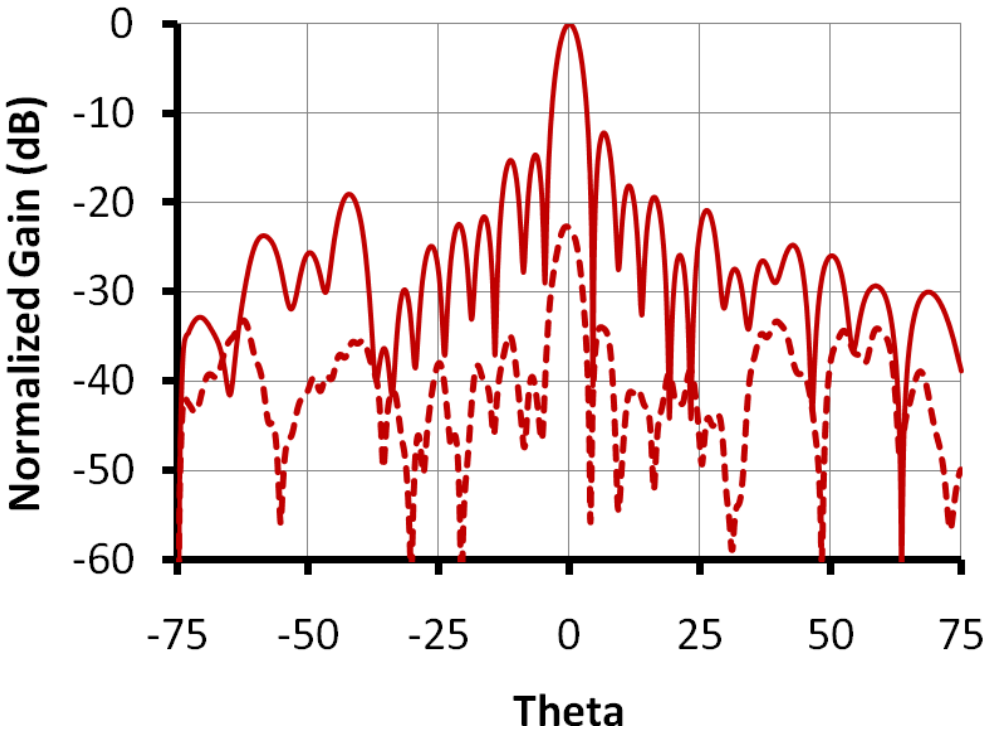


(a)

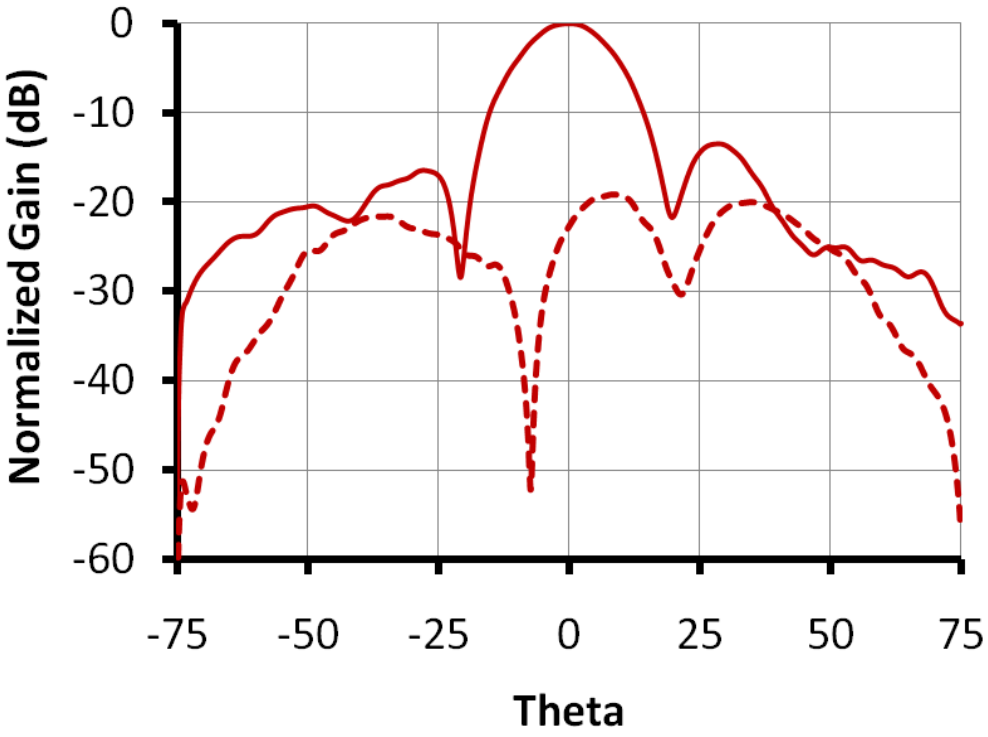


(b)

Figure 5.20 Measured radiation pattern of the full dual-polarized SIW array at 12.2 GHz where $port_2$ (Horizontal pol) is excited and $port_1$ (Vertical pol) is matched. (a) Azimuth cut. (b) Elevation cut.

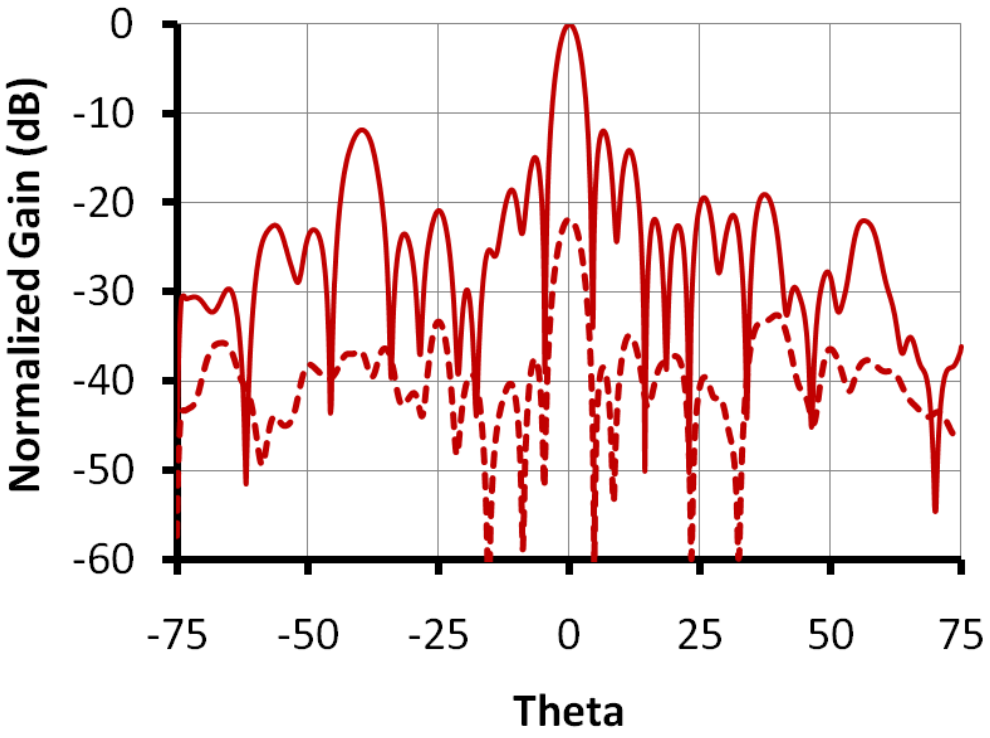


(a)

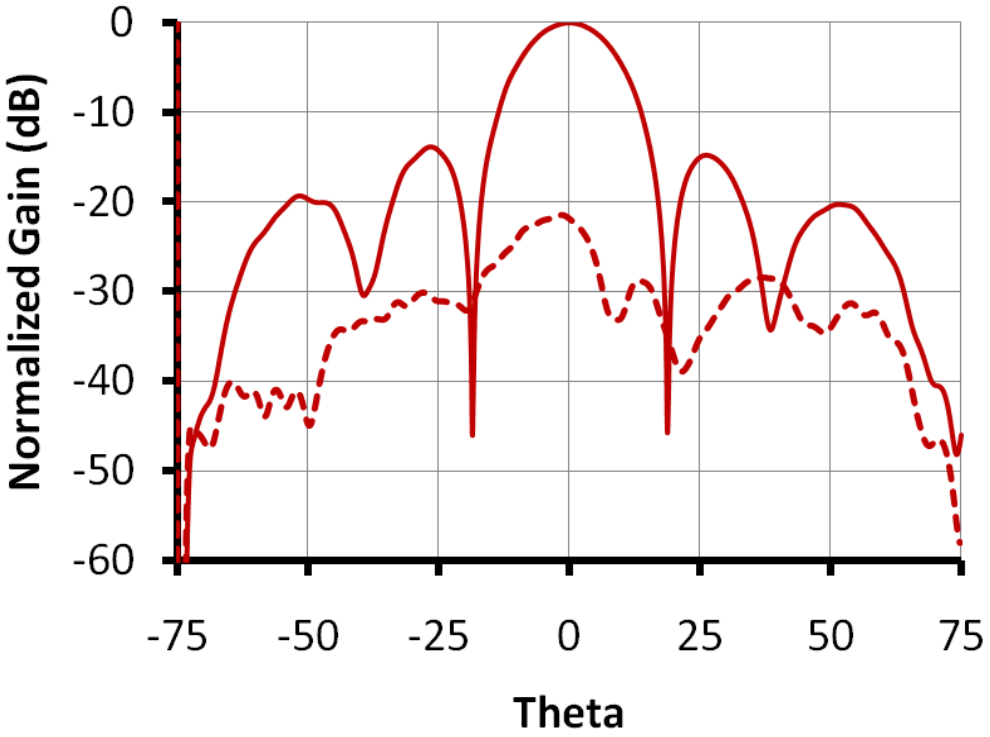


(b)

Figure 5.21 Measured radiation pattern of the full dual-polarized SIW array at 12.2 GHz where $port_1$ (Vertical pol) is excited and $port_2$ (Horizontal pol) is matched. (a) Azimuth cut. (b) Elevation cut.

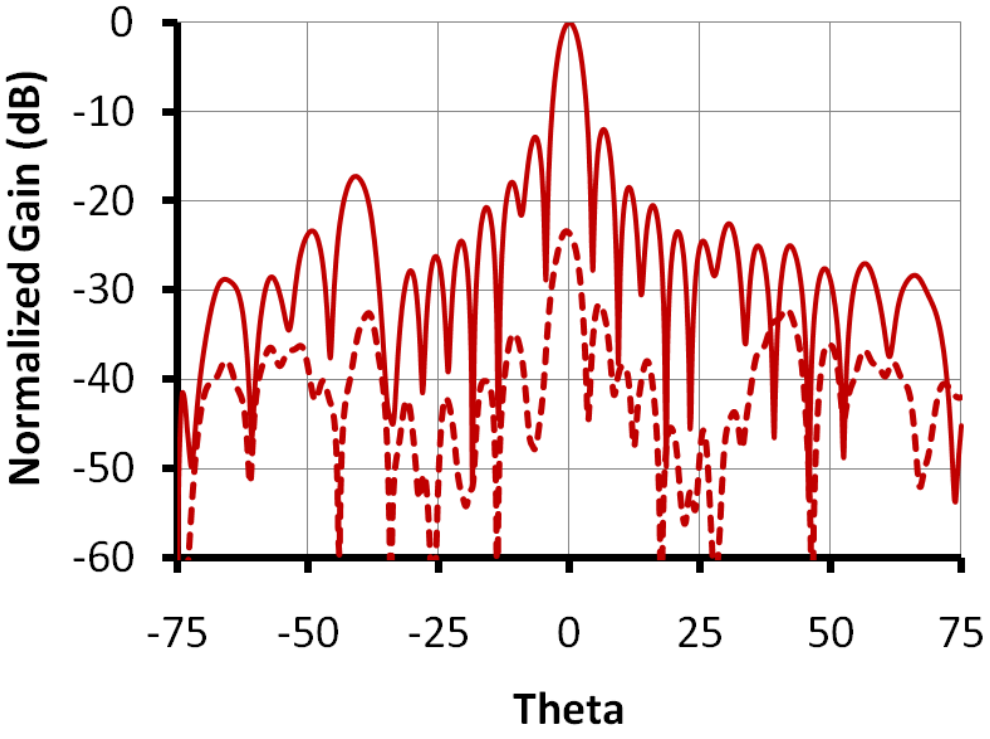


(a)

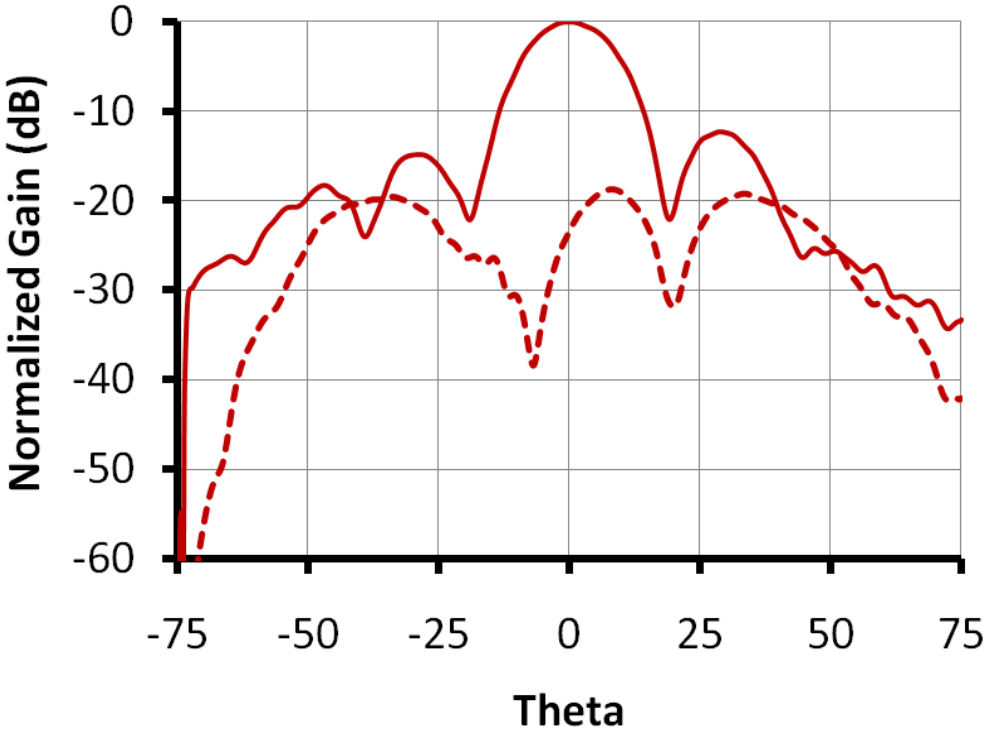


(b)

Figure 5.22 Measured radiation pattern of the full dual-polarized SIW array at 12.45 GHz where $port_2$ (Horizontal pol) is excited and $port_1$ (Vertical pol) is matched. (a) Azimuth cut. (b) Elevation cut.

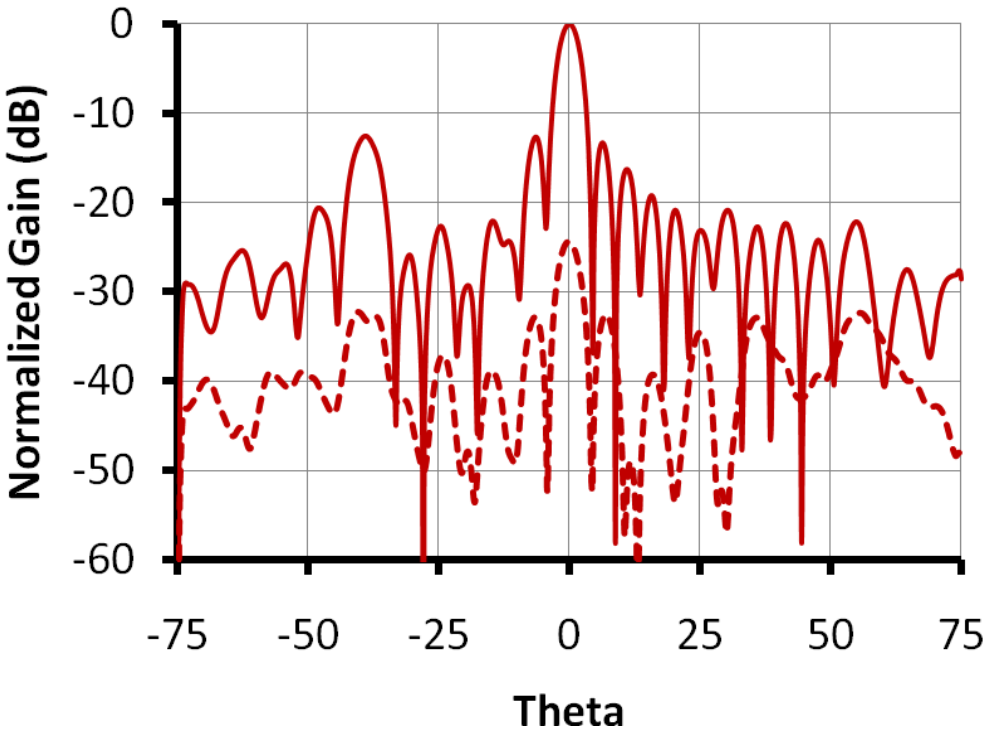


(a)

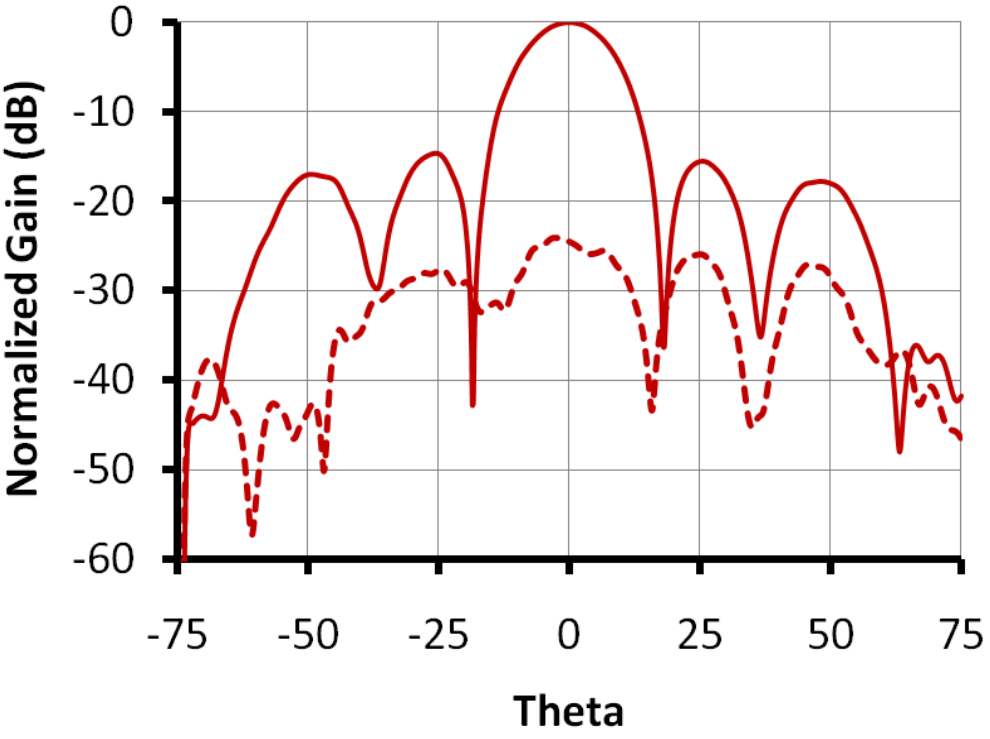


(b)

Figure 5.23 Measured radiation pattern of the full dual-polarized SIW array at 12.45 GHz where $port_1$ (Vertical pol) is excited and $port_2$ (Horizontal pol) is matched. (a) Azimuth cut. (b) Elevation cut.

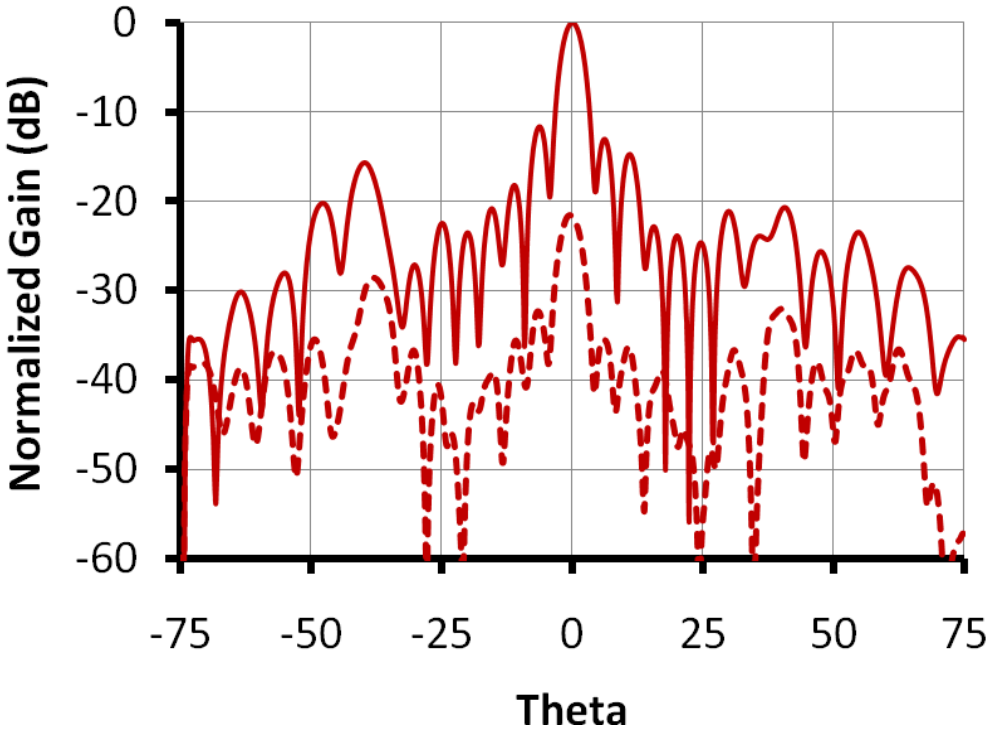


(a)

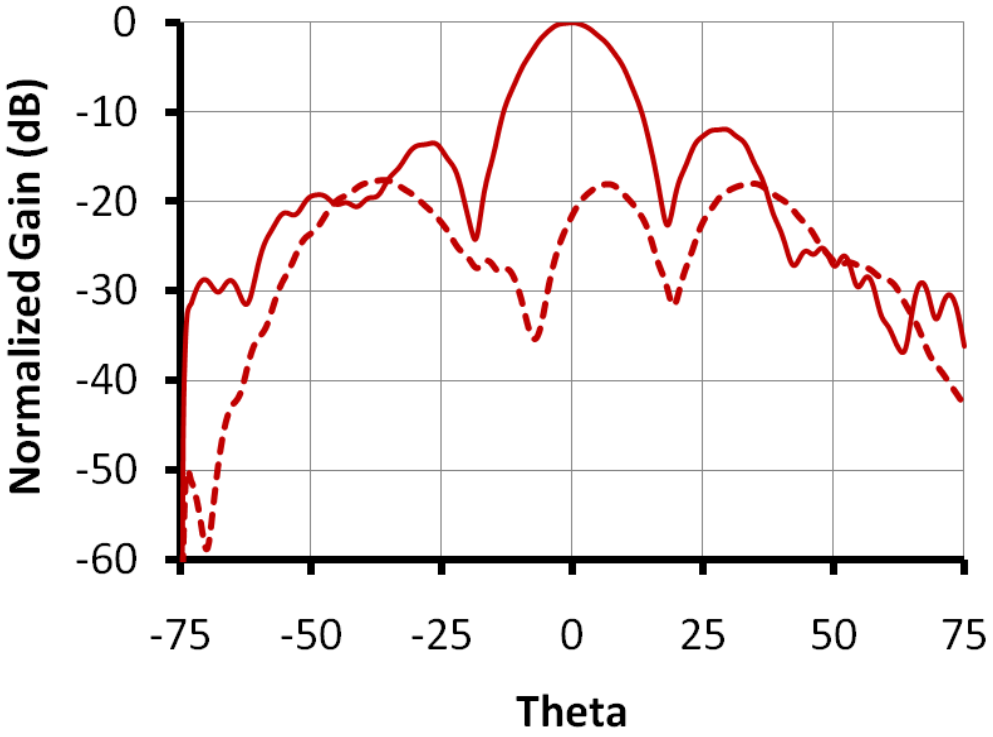


(b)

Figure 5.24 Measured radiation pattern of the full dual-polarized SIW array at 12.7 GHz where $port_2$ (Horizontal pol) is excited and $port_1$ (Vertical pol) is matched. (a) Azimuth cut. (b) Elevation cut.



(a)



(b)

Figure 5.25 Measured radiation pattern of the full dual-polarized SIW array at 12.7 GHz where $port_1$ (Vertical pol) is excited and $port_2$ (Horizontal pol) is matched. (a) Azimuth cut. (b) Elevation cut.

Table 5.3 Summary of the performance of the full dual-polarized array

Frequency	Polarization	Ref(dB)	Gain(dBi)	Gain(dBi)-Matching Correction	Side-Lobe Level (dB)	Cross-Pol Level (dB)
12.20 GHz	Vertical	-9.0	23.97	24.55	-13	-23
12.45 GHz	Vertical	-17.0	24.31	24.40	-13	-24
12.70 GHz	Vertical	-13.5	23.95	24.15	-13	-22
12.20 GHz	Horizontal	-6.0	22.28	23.54	-12	-24
12.45 GHz	Horizontal	-14.4	24.24	24.40	-12	-22
12.70 GHz	Horizontal	-7.0	23.05	24.02	-13	-24

Table 5.4 Summary of losses in the various feed components of the SIW-fed full dual-polarized array

Component	Loss (dB)
Microstrip Feed Loss (2x4)	0.3
Microstrip to Coaxial Transition to SIW	0.2
SIW Feed	0.7
CPW Transition Feed	0.4
SMA Input Connector	0.2
Unaccounted Losses	0.5

5.6 Conclusion

A Ku-band 4x16 cavity-backed microstrip patch array of dual linear/circular polarization has been developed based on substrate integrated waveguide (SIW). The measured antenna array performance covers the DBS frequency range from 12.2 GHz to 12.7 GHz exhibiting about 24.2 dBi, 24.3dBi for the horizontal and vertical polarization, respectively at 12.45 GHz. These results are consistent with the single polarization case and indicate almost the same gain. Poor match at the low frequency end, and

some assembly problem, as we only used metal screws for holding the three layers, caused some gain pattern ripples of over 1 dB, especially at the lower frequency end. Even though, the gain improvement compared to the microstrip case is not significant, but this SIW-fed structure can render dual polarization. In this current design, it is a dual linear polarization, but upon ±90º phasing the feed ports, dual circular polarization could be obtained. The developed array constitutes a good basic panel for larger array designs along with an SIW feed network.

Chapter 6 2-D Analysis of Cavity-Backed Patch Phased Arrays

In this chapter, a simplified 2-D numerical analysis is introduced to analyze phased arrays of cavity-backed patches. The analysis is based on Floquet's theorem to solve a unit cell of the infinite array. The phased array structure is assumed uniform in one direction in order to simplify the analysis to just 2-D, investigating the scan performance only in the E-plane. The rigorous formulation of the problem yields a Fredholm integral equation. Method of moment is then applied to numerically solve the integral equation. Results should shed some light on the potential of using the cavities in widening the scan range of microstrip phased arrays.

6.1 Analysis of Cavity-Backed Patch Phased Arrays

The analysis of infinite phased arrays basically relies on Floquet's theory. Assuming that the array is infinite in extent and is progressively phased and applying the periodic boundary conditions reduces the electrically large array problem to just solving for its unit cell. The goal of this unit cell analysis is to find out the fields and then calculate the active impedance of the phased array. Knowing the active impedance, we can easily calculate the active reflection of the array and so examine the scan performance of the phased array in certain planes of interest; usually the E- and H-planes. The scan performance will show to what scan angle extent the array will still be reasonably matched and if there is any scan blindness.

The scan-blindness in phased arrays is the serious problem of having most of the electromagnetic energy reflected back to the feed source at certain scan angle\s [29]. That scan-blindness problem is very serious in microstrip phased arrays. In fact, the scan blindness severely appears in the relatively thick substrate arrays where the surface waves have more pronounced effects [6, 8]. In that perspective, the cavity-backed patch topology has been suggested by many authors in the literature [10, 38, 47, 94] as an effective approach to impede the surface wave propagation and so eliminate any scan blindness in the scan range of the microstrip patch phased arrays.

Multiple analysis methods have been proposed to tackle the cavity-backed patch phased array problem. One simplification, that helps in having some insight in the problem, while reducing its numerical complexity, is to reduce the 3-D structure to 2-D, assuming uniformity in the third dimension (as in [5], [38]). The 2-D analysis would reveal however, the scan performance only in one plane. Utilizing a 2D finite element analysis Davidovitz, for example, reported in [38], that improved E-plane

scanning performance could be achieved upon using arrays that are built on inhomogeneous substrates. Two types of arrays have been reported. In the first type, the individual strip elements were supported by dielectric slabs of finite extent. In the other type, metallic baffles of substrate-height and finite width are used to isolate the array elements.

On the other hand, an analysis of the radiation properties of infinite phased arrays of probe-fed circular microstrip patches backed by circular cavities using a rigorous Green's function/Galerkin's method have been presented by Zavosh et. al. in [47]. The authors theoretically demonstrated the potential of using the cavities in increasing the scan range of the microstrip phased arrays.

A full-wave method to analyze probe-fed infinite phased arrays of arbitrarily shaped microstrip patches residing in a cavity is proposed by de Aza, et. al. in [94]. The method is based on a combination of the mode matching and finite-element methods (MM-FEM) and provides a rigorous characterization of the coaxial feed. The unit cell is analyzed as an open-ended succession of homogeneous waveguides of diverse cross sections. Each transition between waveguides is solved by a hybrid MM-FEM procedure to obtain its generalized scattering matrix (GSM). Finally, the GSM of the structure, which characterizes the array, is obtained from the individual GSM's by a cascading process. Again, the authors theoretically demonstrated the potential of using the cavities in increasing the scan range of the microstrip phased arrays.

In this chapter, we investigate the cavity-backed patches having in mind the substrate integrated waveguide and targeting to qualitatively demonstrate the scan performance of the cavity-backed structure compared to that of the conventional microstrip phased array. Following the footsteps of Liu, et. al. in [5], we utilize the equivalence principle in the context of a simplified 2D analysis.

6.2 Assumptions and Proposed Analysis Method

To analyze the proposed cavity-backed phased array and develop some basic understanding of its operation, we will start with the special case of probe-fed microstrip patch for simplicity. This problem was previously studied by Liu et al [5, 8], and here we will emphasize on the method of splitting the aperture, the edge-conditions implementation, their convergence evaluation, and their numerical accuracy as they are essential steps in solving the cavity-backed patches case.

We thoroughly investigate Liu's approach for the probe-fed microstrip patch case, but keeping in mind that we need to extend this analysis to the cavity-backed patch case. Additionally, this analysis will be used later to compare the scan performance of the cavity-backed analysis to that of the microstrip array. In this analysis, we will consider only the E-plane scan and frequency performance of a two-dimensional "microstrip-patch" phased array. The 2D analysis should be simpler, and its results should

shed some light on the performance of this array and its main features. Moreover, to simplify the analysis it is inevitable to undertake certain important approximations. On one hand, we first assume that the array is large enough to the point that it is infinite. That approximation potentially simplifies the numerical solution to just analyze a unit cell and subsequently allows us to utilize Floquet's theorem [29]. On the other hand, for the 2D analysis a periodic set of probes are used for the array excitation where filament sheet current excitation are assumed with uniform current distribution in the longitudinal direction, similar to the work done in [5, 7-8].

Mathematically, the patches are replaced by infinitely long strips in one direction, and their probe excitation is replaced by an infinite sheet of current along the same direction, as shown in Figure **6.1**. This representation, however, would seriously cause a numerical challenge. The difficulty encountered in the analysis of probe-fed microstrip patch phased arrays is caused by the presence of longitudinal *(z* directed) feed probes, giving rise to rapidly varying underside patch current distribution in the vicinity of the probes. For a successful numerical solution of the boundary value problems such a singularity must be extracted, as clearly recognized by Liu [5, 8].

We follow Liu's analysis in extracting the sheet (probe) singularity by employing the EM equivalence principle, that permits a breakup of the analysis into that of two simpler problems and in this fashion removes the probe current singularity [5]. The first problem constitutes a feed problem where the probes exist, however the microstrip patches are extended to cover the whole aperture. The second problem is a radiation problem where the probes are removed and the aperture is reopened.

In our analysis (similar to [5]), we will consider z as the-direction of propagation and introduce a Fourier series representation for the unknown aperture electric field distribution, employing Floquet's modes to represent the field in the unit cell, and setting the resulting jump in the magnetic field to the known current distribution on the aperture in the Galerkin's procedure to determine the electric field Fourier coefficients.

6.3 Analysis of Probe-Fed Microstrip Patch Phased Array

Similar to the structure analyzed by [5], as shown in Figure **6.1**(a), the top of a lossless, grounded dielectric substrate slab of thickness ***h,*** small compared to free space wavelength, is periodically coated by perfectly conducting strips of width *a,* spacing *d,* and negligible thickness. The strips are fed by probes, simulated via sheet currents, with uniform density K_0**,** equal to the probe current I_0 divided by the probe spacing d_p in the ***y*** direction. All feed currents are assumed *z* independent, their amplitudes are equal, and their phases are progressive. No *y*- variation is present and the time dependence $e^{j\omega t}$ is suppressed.

The problem will be divided into two simpler ones. Figure **6.1**(a) shows how the probe-fed patch problem could be broken up to two simpler ones using the equivalence principle as suggested by Liu. et. al in [5]. The first problem constitutes a feed problem where the probes exist however; the microstrip patches are extended to cover the whole aperture and the structure is then a parallel plate waveguide, as shown in Figure **6.1**(b). From the feed problem analysis, we can find the current distribution on the upper plate of the parallel-plate waveguide. The second problem is a radiation problem where the probes are removed and the aperture is reopened with an equivalent negative current to that of the feed problem is placed on the aperture, as shown in Figure **6.1**(c).

6.3.1 **Feed Problem**

All feed currents are assumed *z* independent, their amplitudes are equal, and their phases are progressive. No *y* variation is present and the time dependence $e^{j\omega t}$ is suppressed. The solution considers *x* as the direction of propagation, as shown in Figure **6.1**(b), and the solution is obtained in a simple algebraic form.

Assuming a filament probe excitation significantly simplifies the feed problem analysis to just considering the transverse electromagnetic (TEM) mode, which makes the feed problem amenable to transmission line analysis. Floquet's boundary conditions are employed with a phase shift per unit cell δ given by $\delta = k_0 d \sin(\theta)$, where $k_0 = \frac{2\pi}{\lambda_0}$ is the propagation constant in free space, d is the unit cell width, and θ is the scan angle

Figure **6.2** shows the equivalent transmission line model with parameters $Z_1 = Z_0 / \sqrt{\varepsilon_r}$ the characteristic impedance of the line and $k = k_0\sqrt{\varepsilon_r}$ the propagation constant on the line, and ε_r the relative permittivity of the substrate.

In order to find the current distribution along the transmission line, the model in Figure **6.2** can be simply analyzed assuming unknown voltages and currents at each node of the unit cell from x=0 to x=d. However, those currents and voltages could be written easily in terms of the incident v_i^+, reflected v_i^- voltages, and the characteristic impedance of each transmission line section of the two sections constituting the unit cell. That reduces the model to four equations that could be written in a matrix form as

$$Ax = b \tag{6-1}$$

Where

$$A = \begin{pmatrix} e^{-jkx'} & e^{jkx'} & -1 & -1 \\ e^{-jkx'} & -e^{jkx'} & -1 & 1 \\ 1 & 1 & -e^{-j[k(d-x')-\delta]} & -e^{j[k(d-x')+\delta]} \\ 1 & -1 & -e^{-j[k(d-x')-\delta]} & e^{j[k(d-x')+\delta]} \end{pmatrix}$$

and

$$x = \begin{pmatrix} v_1^+ \\ v_1^- \\ v_2^+ \\ v_2^- \end{pmatrix}, \qquad b = \begin{pmatrix} 0 \\ -I_0 Z_1 \\ 0 \\ 0 \end{pmatrix}$$

Where I_o is the current amplitude of the sheet current and Z_1 is the characteristic impedance of the equivalent transmission line

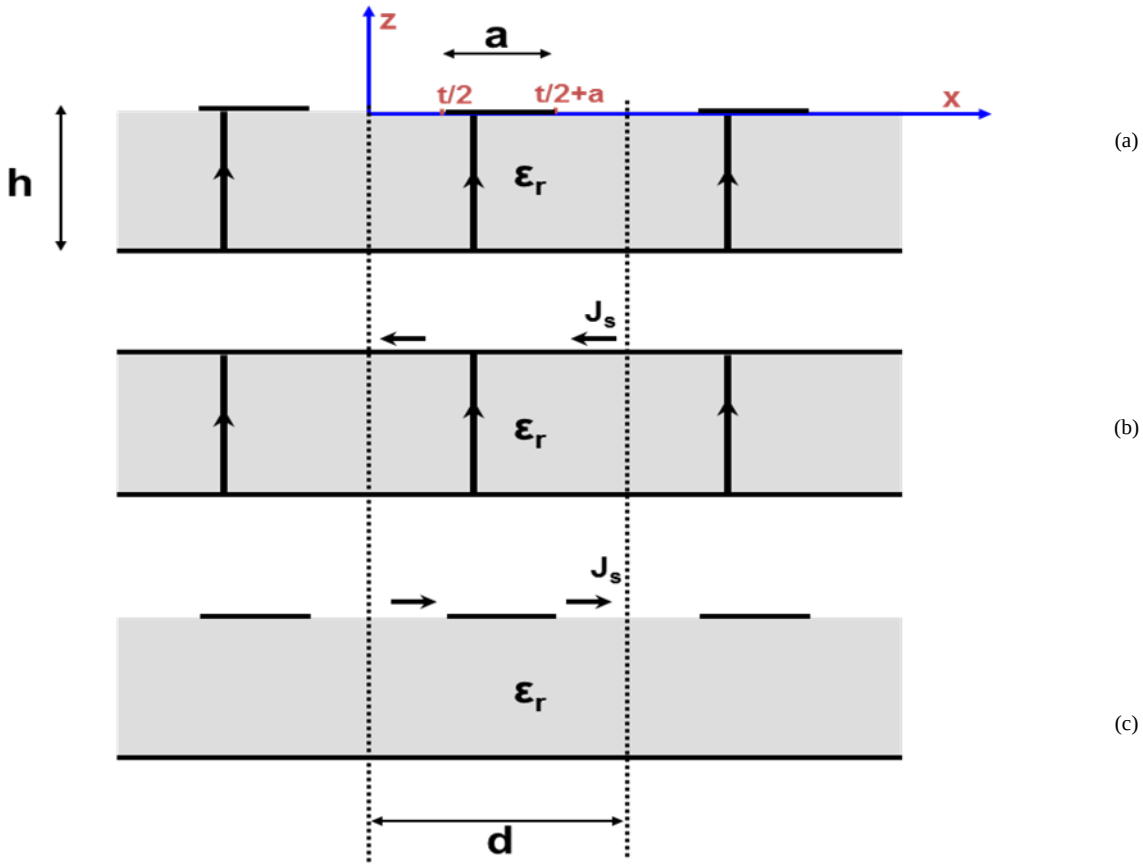


Figure 6.1 Phased array of probe-fed patches (a) Simplified 2-D problem. (b) Equivalent feed problem. (c) Equivalent radiation problem.

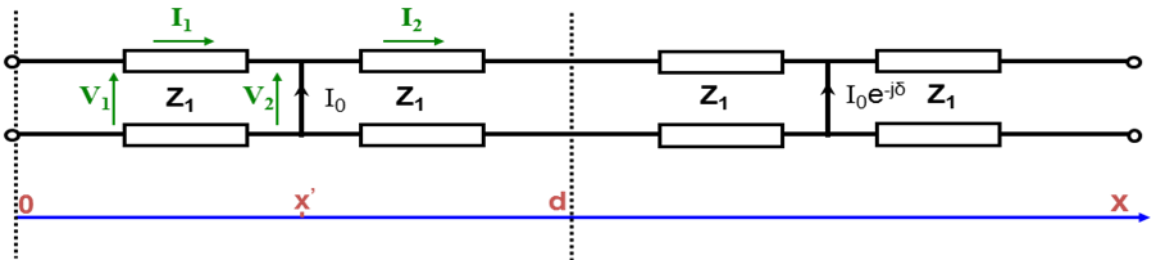


Figure 6.2 Transmission line model of the feed problem of the microstrip phased array.

Resulting in

$$I(x)=\begin{cases}\dfrac{I_0}{2}\left[\dfrac{e^{-j\delta-jk(x-x')}}{e^{-j\delta}-e^{-jkd}}-\dfrac{e^{-jk(d-x+x')}}{e^{j\delta}-e^{-jkd}}\right], x'<x<d\\ \dfrac{I_0}{2}\left[\dfrac{e^{-jk(d+x-x')}}{e^{-j\delta}-e^{-jkd}}-\dfrac{e^{j\delta+jk(x-x')}}{e^{j\delta}-e^{-jkd}}\right], 0<x<x'\end{cases} \tag{6-2}$$

Where x' is the sheet current position with respect to x axis

6.3.2 **Radiation Problem**

Regarding the radiation problem unit cell, shown in Figure **6.3**, the numerical solution of the boundary value problem could be divided into two regions, as shown in Figure **6.3**. In each region the field could be expanded in terms of the corresponding basis modes of the region. First the fields in region I could be expanded in terms of the Floquet's basis modes as follows

$$E_x^I(x,z)=\sum_{m=-\infty}^{\infty}V_m\Psi_m(x)\sin\left(\beta_{zm}(z+h)\right) \tag{6-3a}$$

$$H_y^I(x,z)=\sum_{m=-\infty}^{\infty}jY_mV_m\Psi_m(x)\cos\left(\beta_{zm}(z+h)\right) \tag{6-3b}$$

Where

$$\Psi_n(x)=\frac{1}{\sqrt{d}}e^{-jK_{xm}(x-x_o)}$$

$$K_{xm}=\frac{2m\pi+\delta}{d},\quad k=k_0\sqrt{\varepsilon_r},\quad Y_m=\frac{\omega\varepsilon_0\varepsilon_r}{\beta_{zm}}$$

$$\beta_{zm} = \begin{cases} \sqrt{k^2 - K_{xm}{}^2} & k^2 \geq K_{xm}{}^2 \\ -j\sqrt{K_{xm}{}^2 - k^2} & k^2 < K_{xm}{}^2 \end{cases}$$

Similarly, the fields could be expanded in Region II as

$$E_x^{II}(x,z) = \sum_{m=-\infty}^{\infty} V_m \Psi_m(x) e^{-j\xi_{mz} z} \tag{6-4a}$$

$$H_y^{II}(x,z) = \sum_{m=-\infty}^{\infty} Y_m V_m \Psi_m(x) e^{-j\xi_{mz} z} \tag{6-4b}$$

Where

$$Y_m = \frac{\omega \varepsilon_0 \varepsilon_r}{\xi_{mz}}$$

$$\xi_{mz} = \begin{cases} \sqrt{k_0{}^2 - K_{xm}{}^2} & k_0{}^2 \geq K_{xm}{}^2 \\ -j\sqrt{K_{xm}{}^2 - k_0{}^2} & k_0{}^2 < K_{xm}{}^2 \end{cases}$$

Meanwhile, the fields on the aperture could be expanded in terms of left and right aperture basis

$$E_a^-(x,0^-) = E_a^+(x,0^+) = E_l + E_r \tag{6-5}$$

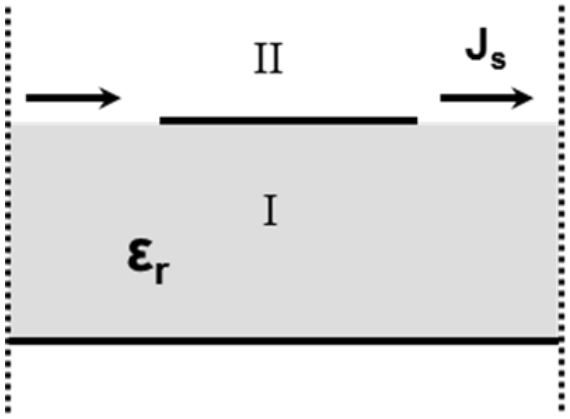


Figure 6.3 Radiation problem unit cell of the microstrip phased array.

Such that

$$E_l = \sum_{i=0}^{\infty} a_i \Phi_i(x)$$

$$E_r = \sum_{i=0}^{\infty} b_n \Phi_n(x)$$

Where

$$\Phi_n(x) = \begin{cases} \dfrac{\cos\left(\dfrac{2n\pi}{t}\cdot x\right)}{\sqrt{1-\left(\dfrac{2x}{t}\right)^2}} & 0 \le x \le t/2 \\ 0 & \textit{elsewhere} \end{cases}$$

and

$$\Phi_n(x) = \begin{cases} \dfrac{\cos\left(\dfrac{2n\pi}{t}\cdot(d-x)\right)}{\sqrt{1-\left(\dfrac{2(d-x)}{t}\right)^2}} & t/2 + a \le x \le d \\ 0 & \textit{elsewhere} \end{cases}$$

Upon matching the electric-field on both sides of the aperture, we end up with

$$\sum_{i=0}^{\infty} a_i \Phi_i(x) + \sum_{n=0}^{\infty} b_n \Phi_n(x) = \sum_{m=-\infty}^{\infty} V_m \Psi_m(x) \sin(\beta_{zm} h) = \sum_{m=-\infty}^{\infty} V_m \Psi_m(x) \qquad (6\text{-}6)$$

Taking an inner product of eq.(6-6) with $\Psi_p^*(x)$ leads us to the following

$$V_p = V_p \sin(\beta_{zp} h) = \sum_{i=0}^{\infty} a_i f_{ip}^* + \sum_{n=0}^{\infty} b_n g_{np}^* \qquad (6\text{-}7)$$

Where

$$f_{ip}^* = \int_{SL} \Phi_i(x).\Psi_p^*(x)dx$$

$$g_{np}^* = \int_{SR} \Phi_n(x).\Psi_p^*(x)dx$$

and SL is the left aperture domain $0 \le x < t/2$ and SR is the right aperture domain $a + t/2 \le x < d$

On the other hand upon matching the magnetic field on both sides of the aperture, we end up with

$$J_s(x) = \sum_{m=-\infty}^{\infty} \left(Y_m - Y_m \cot\left(\beta_{zm} h\right)\right) V_m \Psi_m(x) \tag{6-8}$$

Then substituting for V_p from eq.(6-7) in eq.(6-8) leads to

$$J_s(x) = \sum_{m=-\infty}^{\infty} \left(Y_m - Y_m \cot\left(\beta_{zm} h\right)\right) \Psi_m(x) \left(\sum_{i=1}^{\infty} a_i f_{im}^* + \sum_{n=1}^{\infty} b_n g_{nm}^* \right) \tag{6-9}$$

Testing the eq. (6-9) by $\Phi_q(x)$ results in

$$\vartheta_q = \sum_{n=0}^{\infty} \sum_{m=-\infty}^{\infty} f_{qm} \left(Y_m - Y_m \cot\left(\beta_{zm} h\right)\right) \left(\sum_{i=0}^{\infty} a_i f_{im}^* + \sum_{n=0}^{\infty} b_n g_{nm}^* \right) \tag{6-10}$$

Where

$$\vartheta_p = \int_{SL} J_s(x).\Phi_p(x) dx$$

Which could be written in a matrix form as

$$\mathbf{J = FCF^* a + FCG^* b} \tag{6-11a}$$

Where

$$\mathbf{C} = diag\left(Y\right) - diag\left(Y.\cot\left(\beta_z h\right)\right)$$

Similarly by testing eq.(6-9) with $\Phi_q(x)$, we end up with a second matrix equation

$$\mathbf{J = GCF^* a + GCG^* b} \tag{6-11b}$$

Where

$$\vartheta_p = \int_{SR} J_s(x).\Phi_p(x) dx$$

By solving the two matrix equations (6-11a) and (6-11b), we can find the coefficient vectors *a* and *b*, then we can find the voltage coefficients V using eq. (6-7).

6.3.3 **Active Impedance**

The active impedance of the probe-fed microstrip phased array could be calculated following the definition of Liu in [5]

$$Z_a = \int_{-h}^{0} \frac{E_z dz}{K_0 d_p} \tag{6-12}$$

Where d_p is the probe spacing in the uniform direction which should not exceed $\lambda_0/2$**,** a spacing of $\lambda_0/3$ (at midband) was used. Applying the active impedance integral results in, similar to [5]

$$Z_a = -j\,\frac{Z_0 \sin(kd)}{2\left(\cos(kd)-\cos(\delta)\right)} + \frac{1}{I_0\sqrt{d}} \sum_{m=-\infty}^{\infty} V_m \frac{K_{xm} Y_m}{\omega \varepsilon_r \beta_{zm}} e^{-jk_{xm}x'} \tag{6-13}$$

Where V_m are the voltage coefficients of the Floquet's modes (calculated from radiation problem; section 6.2.2), and the series will be truncated to M terms in the numerical solution.

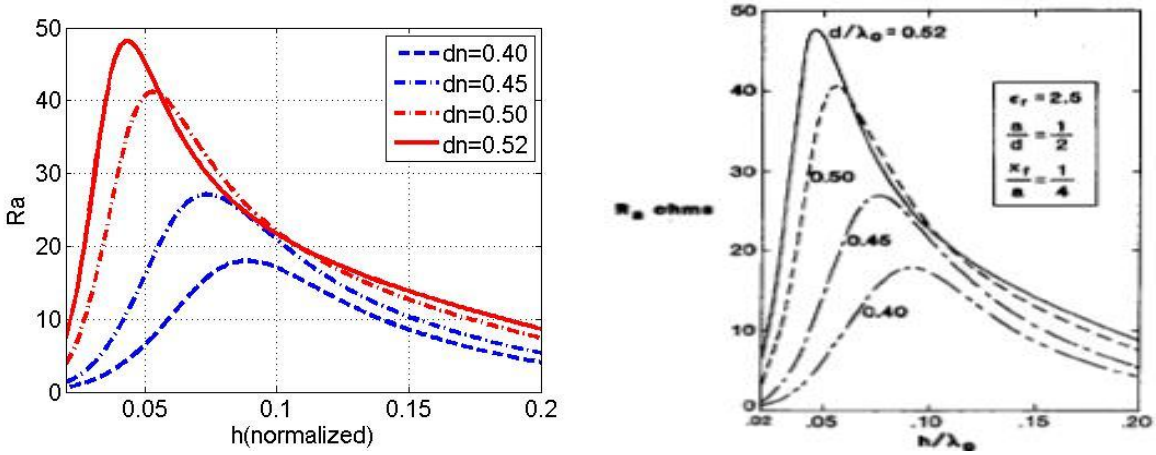
6.3.4 **Numerical Results**

The analysis of the probe-fed patch phased array along with the edge condition were coded and numerically verified against [5], as shown in Figure 6.4, (similar to Figs 3 and 4 in [5]) in case of ε_r=2.5, and x_f=a/4. Figure 6.4 shows the active resistance versus the normalized substrate thickness for various patch and unit cell widths. Good agreement is obtained between our results and Liu's ones.

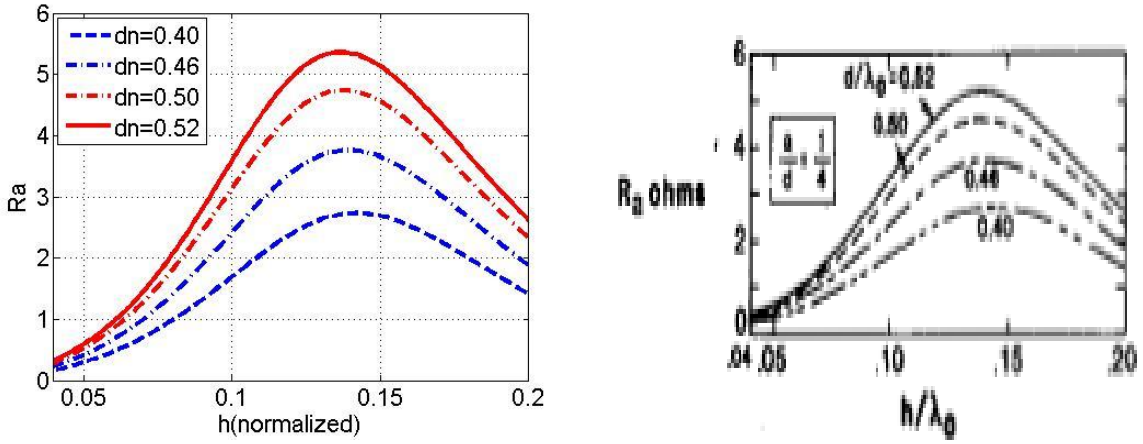
Figure 6.5 shows surface current numerically calculated from the feed problem, assuming 1 mA current excitation on the probes, and in case of ε_r=2.5**,** d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0. The real part of the current has been verified to have that 1 mA discontinuity at the probe location.

A through convergence study have been carried out in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0 to determine the proper values for N (number of basis modes) and M (number of Floquet modes) to truncate their respective series. Initially N was kept constant (equal to 5), while M was changed and the active resistance and reactance were numerically calculated, as shown in Figure 6.6. Our convergence study have shown that M>40N is needed to reach satisfactory convergence for the active element parameters. On the other hand, and as expected, the convergence of the implemented edge basis is much faster than that of the edge-less basis used by [5], as demonstrated in Figure 6.7, where only N=5 is needed to reach convergence in case of edge-basis compared to N>20 in case of the edge-less basis.

The aperture field numerically calculated from the radiation problem, in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0, is shown in Figure 6.8 for various values of N and M demonstrating the field behavior nearby the edge and showing the field matching between the one calculated from the basis sum (shown in blue) and the one calculated from the Floquet's sum (shown in red).



(a)



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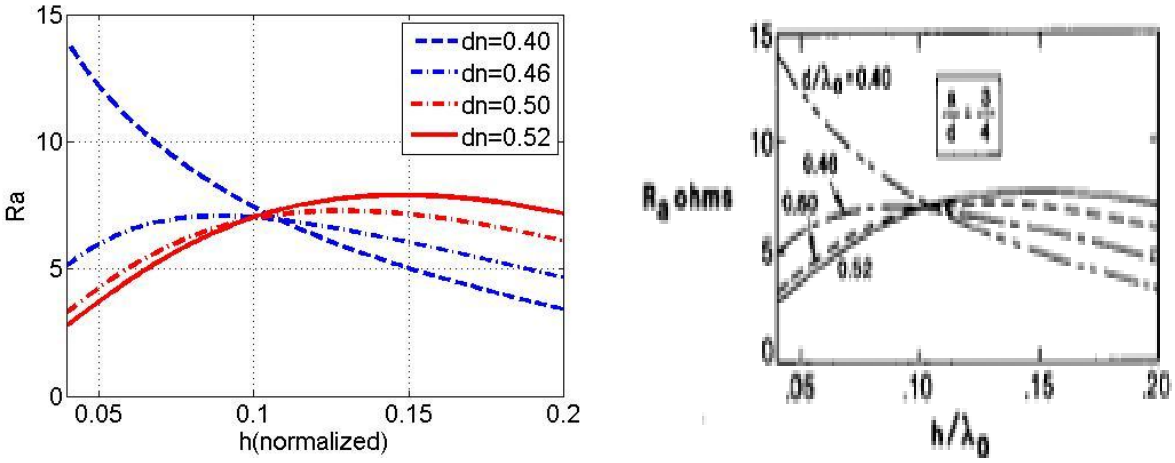


(c)

Figure 6.4 Active resistance of the microstrip phased array in case of ε_r=2.5, and x_f=a/4. (a) a=d/2. (b) a=d/4. (c) a=3d/4 (dn=d/λ_0 the obtained numerical results are obtained using cos-basis and assuming N=10, M=44).

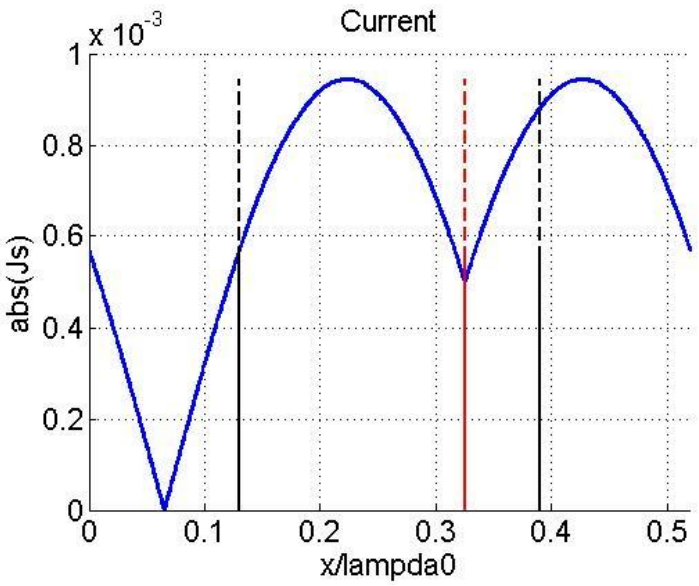
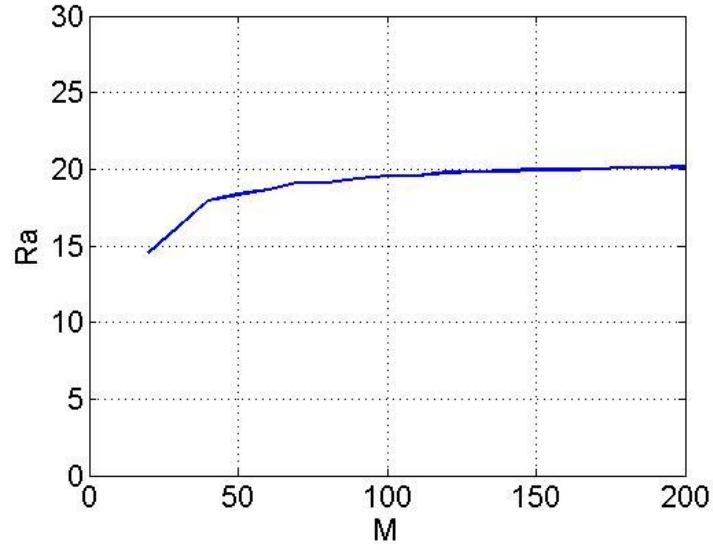
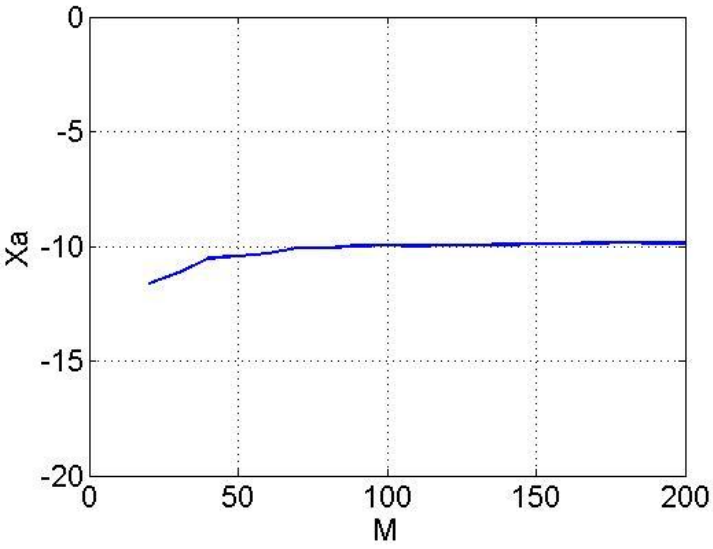


Figure 6.5 Surface current (A/m) calculated from the feed problem for the microstrip phased array in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0.

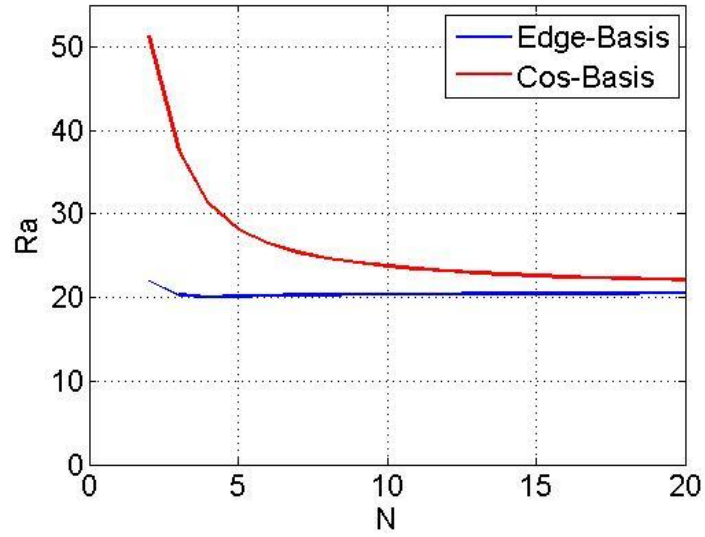


(a)

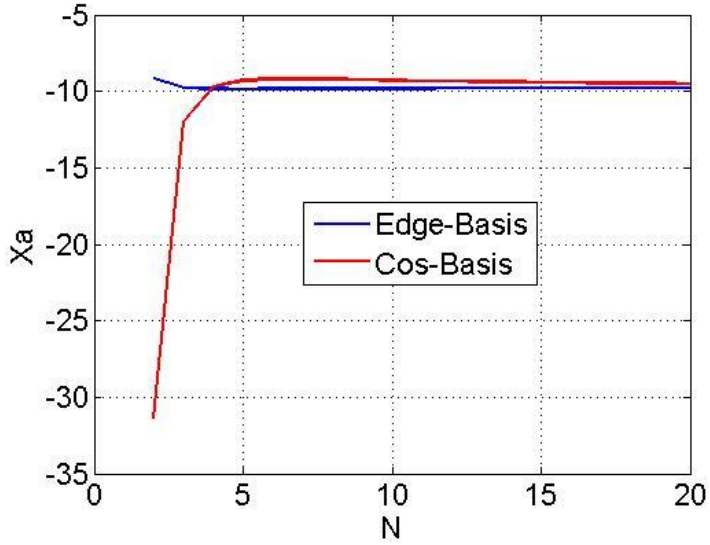


(b)

Figure 6.6 Convergence behavior of the numerically calculated active impedance vs. the number of Floquet's modes for the microstrip phased array in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0. (a) Active resistance. (b) Active reactance.

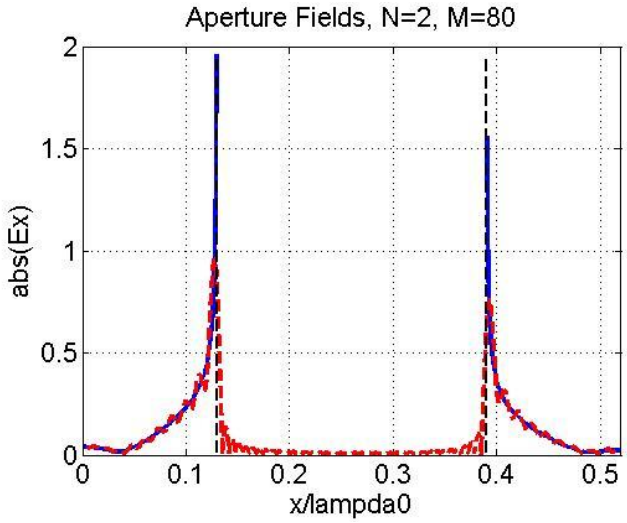


(a)

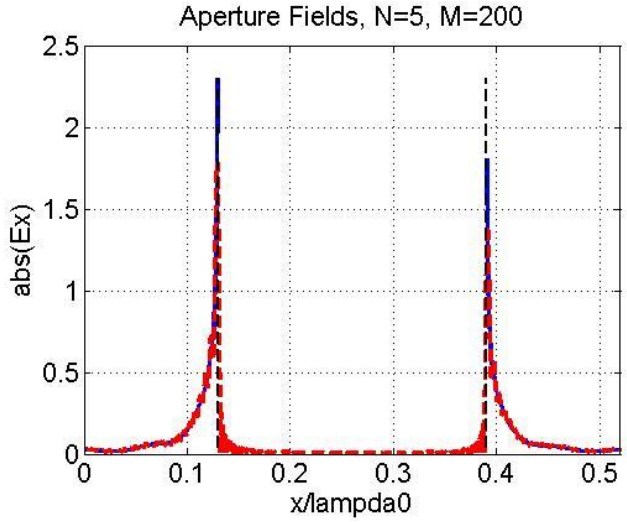


(b)

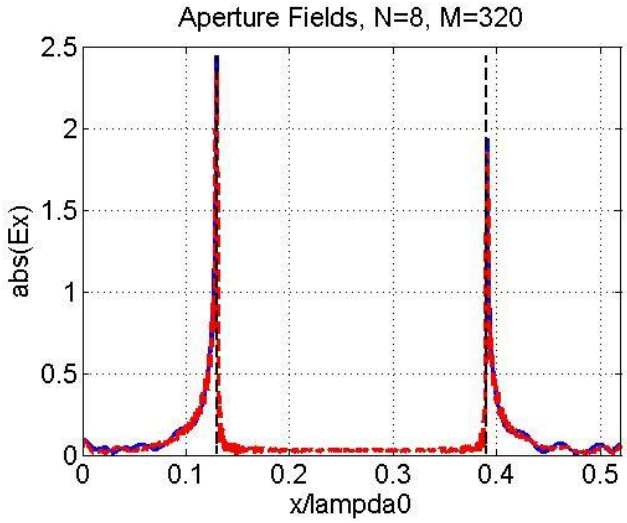
Figure 6.7 Convergence study showing the numerically calculated active impedance vs. the number of basis modes for the microstrip phased array in case of $d=0.52\lambda_0$, $a=d/2$, $x_f=a/4$, and $h=0.03\lambda_0$. (a) Active resistance. (b) Active reactance.



(a)



(b)

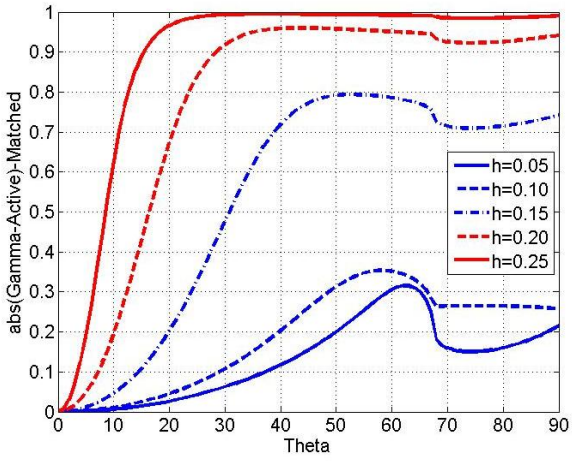


(c)

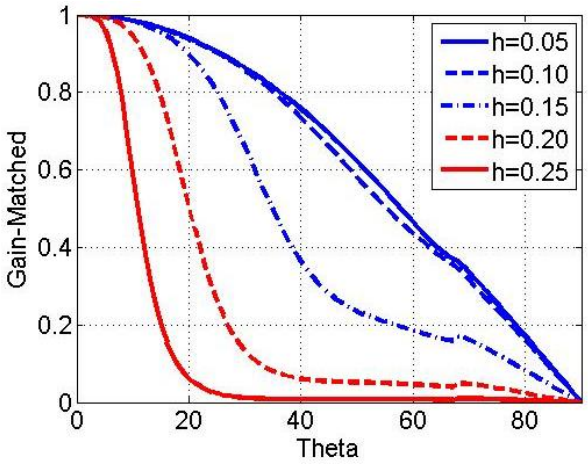
Figure 6.8 Aperture field calculated from the radiation problem of the microstirp phased array in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0 from both the basis sum in blue and the Floquet's sum in red. (a) N=2, M=80. (b) N=5, M=200. (c) N=8, M=320.

The E-plane scan performance of the probe fed microstrip array in case of ε_r=2.5, d=0.52λ_0, a=d/2, and x_f=a/4 is shown in Figure 6.9, compared to that demonstrated before by Liu, et. al. in [5], for various substrate thicknesses. The array was broadside matched to 50Ω like [5] based on $Z_{a-matched} = \left(Z_a + Z_B{}^*\right).50/\left(2.real\left(Z_B\right)\right)$, where Z_B is the active impedance at broadside. As expected, despite that thicker substrate will secure wider bandwidth it will lead to seriously narrower scan performance [5-9, 67, 95-96].

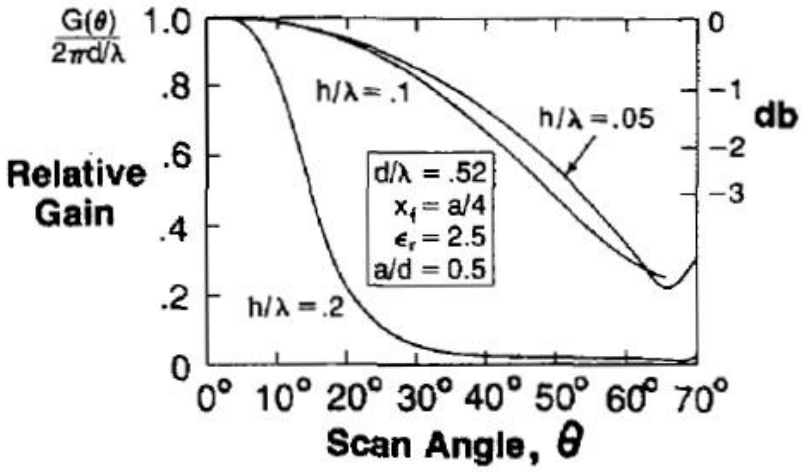
A comparison between the simulated aperture field obtained from HFSS and the numerically calculated one, in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0, is shown in Figure 6.10 demonstrating the validity of the proposed numerical approach and the suitability of commercial codes (HFSS) in analyzing such probe-fed structures. Very good agreement exists between the numerically calculated field and the HFSS simulated one.



(a)

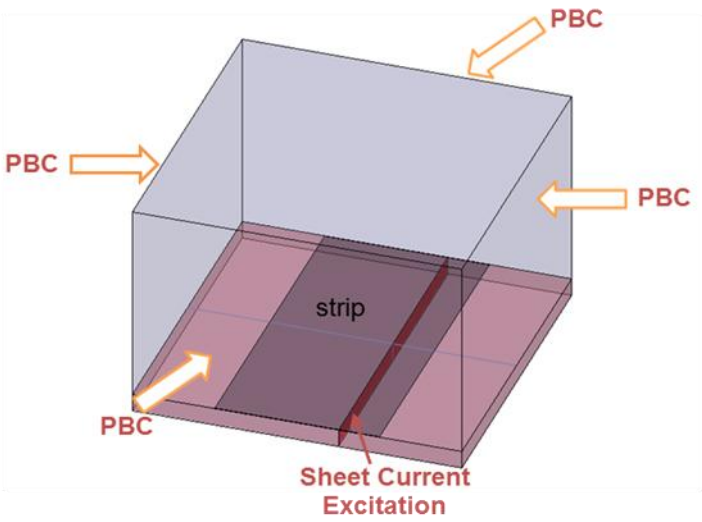


(b)

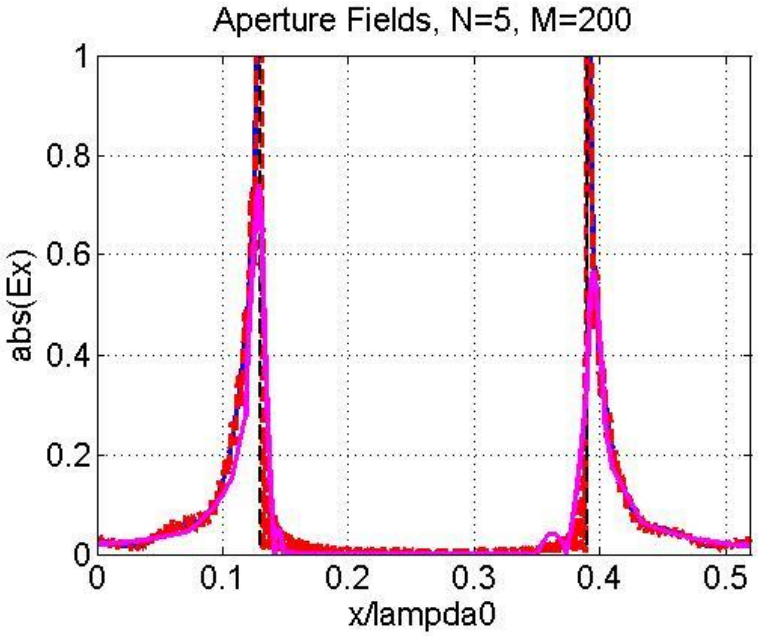


(c)

Figure 6.9 E-plane matched active reflection and gain performance versus scan angle for the microstrip phased array in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0. (a) Matched active reflection coefficient. (b) Calculated matched active gain. (c) Matched gain of Liu, et. al. in [5].



(a)



(b)

Figure 6.10 Simulation comparison to HFSS for the microstrip phased array (a) HFSS Model. (b) HFSS aperture field in magenta vs. the numerically calculated one in red in case of ε_r=2.5, d=0.52λ_0, a=d/2, x_f=a/4, and h=0.03λ_0.

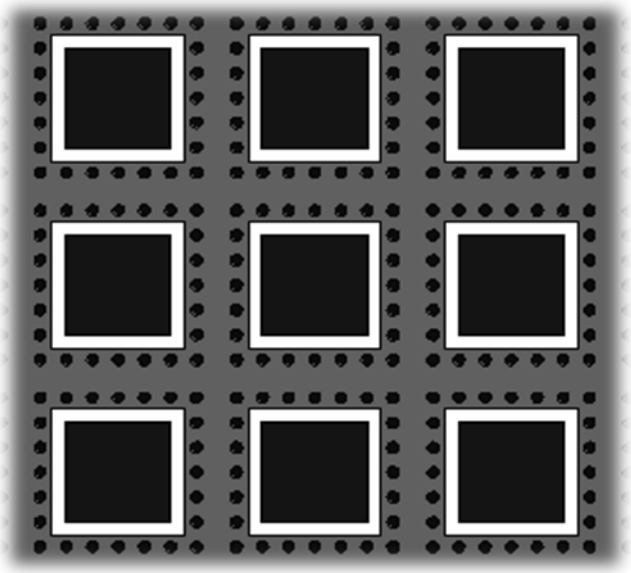
6.4 Analysis of Probe-Fed Cavity-Backed Patch Phased Array (Case of Two Substrates)

The phased array of cavity-backed microstrip patches (case of two substrates) is simply comprised of a stack of two substrates, namely: a microstrip substrate of dielectric constant ε_{rs} and height h_s, and a cavity substrate of dielectric constant ε_{rc} and height h_c, as shown in Figure 6.11(b). Patches of side length *a* are printed on the microstrip substrate while being fed through probes going all the way along the two substrates. The ground of the microstrip substrate and the top layer of the cavity substrate have openings of side length *2R* underneath the patches. Many via holes spaced along the openings are laser-drilled in the cavity substrate and are then platted-through constituting the SIW rectangular cavities backing the patches, as shown in Figure 6.11(a).

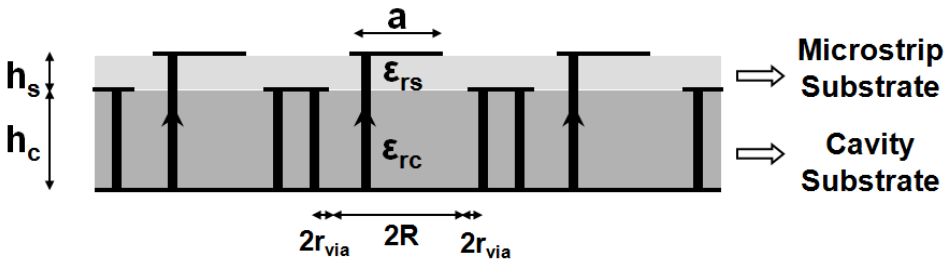
It is worth mentioning also that keeping the same material for both substrates would maintain a good thermal expansion matching between the two substrates. Thus, we will assume the same material of dielectric constant ε_r for the two substrates.

We have replaced the SIW walls by continuous metal walls of equivalent side length W_c, as shown in Figure 6.12. This approximation is justified by the fact that the SIW walls with via holes spaced closely ~ $\lambda_g/10$ will sufficiently confine all the electromagnetic energy within it. Finding such equivalence between SIW and the solid wall cavity has been discussed previously in Chapter 2, for single elements antennas.

Following the analysis theme, we have used for the microstrip patch phased array in the previous section, the problem could be analyzed utilizing the equivalence principle, where it could be divided into two separate problems; feed problem and radiation problem as shown in Figure 6.12(b) and (c), respectively.



(a)



(b)

Figure 6.11 Proposed phased array of SIW cavity-backed microstrip patches (case of two substrates). (a) Top view. (b) Side view.

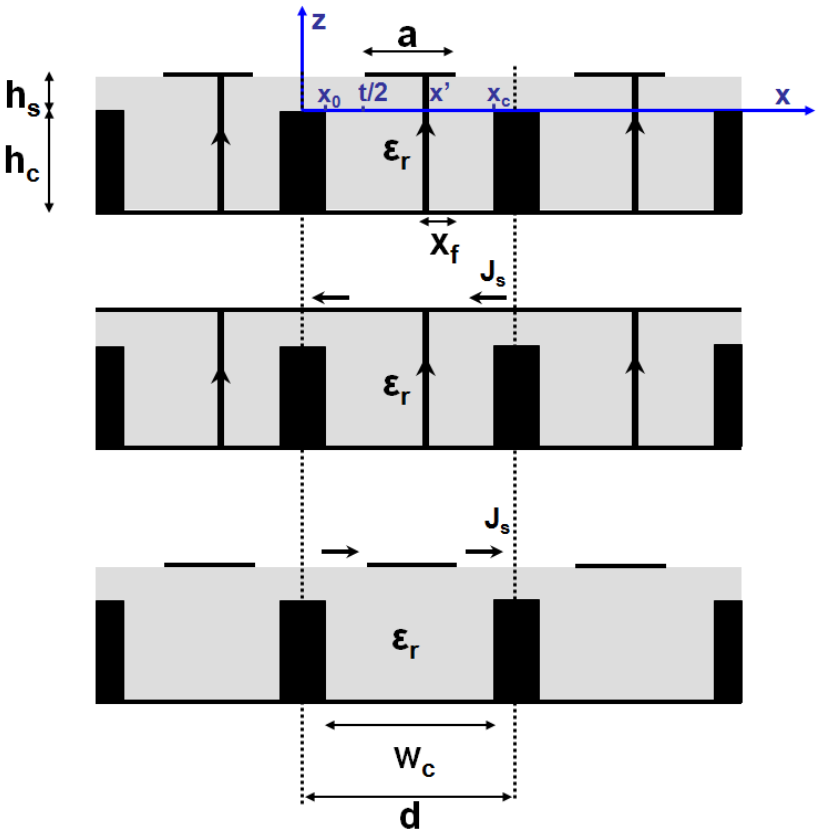


Figure 6.12 SIW phased array of cavity-backed patches (case of two substrates) (a) Simplified 2-D problem. (b) Equivalent feed problem. (c) Equivalent radiation problem.

6.4.1 **Feed Problem**

Again assuming filament probe excitation relatively simplifies the feed problem analysis to just considering the transverse electromagnetic (TEM) mode which makes the feed problem amenable to transmission line analysis. Figure 6.13 shows the equivalent transmission line model where Z_1 and Z_2 denote the characteristic impedance of the parallel plate waveguide; off-cavity, and in-cavity regions, respectively, such that

$$Z_1 = \frac{Z_0 h_s}{\sqrt{\varepsilon_r} L_y},$$

$$Z_2 = \frac{Z_0 (h_s + h_c)}{\sqrt{\varepsilon_r} L_y}$$

Where L_y is the length of the unit cell in the uniform direction (has been set to unity).

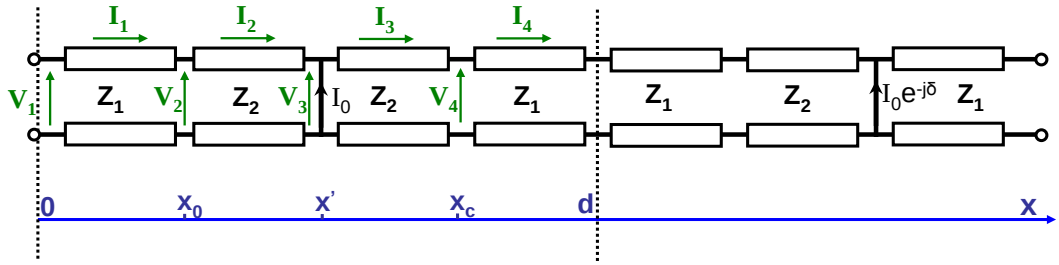


Figure 6.13 Transmission line model of the feed problem of the cavity-backed phased array (case of two substrates).

In order to find the current distribution along the transmission line, the transmission line model was simply analyzed assuming unknown voltage and current at each node of the unit cell from x=0 to x=d (there are four nodes at $x=x_0$, $x=x'$, $x=x_c$, and x=d, as shown in Figure 6.13).

These currents and voltages could be written easily in terms of the incident v_i^+, reflected v_i^- voltages, and the characteristic impedance of each transmission line section of the four sections that constitutes the unit cell reducing the model to eight equations that could be written in a matrix form as

$$Ax = b \tag{6-14}$$

Where

$$A = \begin{pmatrix} e^{-jkx_o} & e^{jkx_o} & -1 & -1 & 0 & 0 & 0 & 0 \\ e^{-jkx_o} & -e^{jkx_o} & -Z_1/Z_2 & Z_1/Z_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & e^{-jk(x'-x_o)} & e^{jk(x'-x_o)} & -1 & -1 & 0 & 0 \\ 0 & 0 & e^{-jk(x'-x_o)} & -e^{jk(x'-x_o)} & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & e^{-jk(x_c-x')} & e^{jk(x_c-x')} & -1 & -1 \\ 0 & 0 & 0 & 0 & e^{-jk(x_c-x')} & -e^{jk(x_c-x')} & -Z_2/Z_1 & Z_2/Z_1 \\ 1 & 1 & 0 & 0 & 0 & 0 & -e^{-j[k(d-x_c)-\delta]} & -e^{j[k(d-x_c)+\delta]} \\ 1 & -1 & 0 & 0 & 0 & 0 & -e^{-j[k(d-x_c)-\delta]} & e^{j[k(d-x_c)+\delta]} \end{pmatrix}$$

$$x = \begin{pmatrix} \mathrm{v}_1^+ \\ \mathrm{v}_1^- \\ \mathrm{v}_2^+ \\ \mathrm{v}_2^- \\ \mathrm{v}_3^+ \\ \mathrm{v}_3^- \\ \mathrm{v}_4^+ \\ \mathrm{v}_4^- \end{pmatrix} \qquad b = \begin{pmatrix} 0 \\ 0 \\ 0 \\ -I_0 Z_2 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

By solving eq. (6-14) we can find the incident and reflected voltages, and then we can find the current on the transmission line as

$$I(x) = \begin{cases} \dfrac{\mathrm{v}_1^+}{Z_1} e^{-jkx} - \dfrac{\mathrm{v}_1^-}{Z_1} e^{jkx} & 0 \le x < x_o \\ \dfrac{\mathrm{v}_2^+}{Z_2} e^{-jk(x-x_o)} - \dfrac{\mathrm{v}_2^-}{Z_2} e^{jk(x-x_o)} & x_o \le x < x' \\ \dfrac{\mathrm{v}_3^+}{Z_2} e^{-jk(x-x')} - \dfrac{\mathrm{v}_3^-}{Z_2} e^{jk(x-x')} & x' \le x < x_c \\ \dfrac{\mathrm{v}_4^+}{Z_1} e^{-jk(x-x_c)} - \dfrac{\mathrm{v}_4^-}{Z_1} e^{jk(x-x_c)} & x_c \le x < d \end{cases} \tag{6-15}$$

6.4.2 **Radiation Problem**

Regarding the radiation problem unit cell, the numerical solution of this boundary value problem could be divided into three regions as shown in Figure 6.14. In each region the field could be expanded in terms of the corresponding region basis modes. First the fields in region I could be expanded in terms of the waveguide basis modes as following

$$E_x^I(x,z) = \sum_{n=0}^{\infty} v_n \Phi_n(x) \sin\left(\beta_n (z + h_c)\right) \tag{6-16a}$$

$$H_y^I(x,z) = \sum_{n=0}^{\infty} j v_n y_n \Phi_n(x) \cos\left(\beta_n (z + h_c)\right) \tag{6-16b}$$

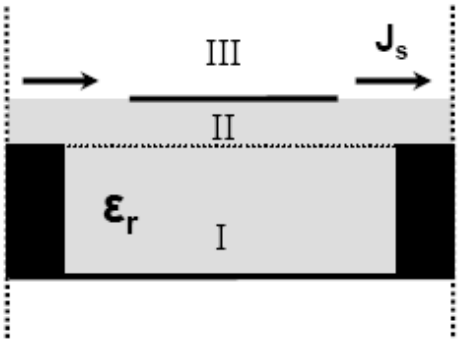


Figure 6.14 Radiation problem unit cell of the cavity-backed phased array (case of two substrates).

Where

$$\Phi_n(x)=\begin{cases}\sqrt{\dfrac{2}{w_c}}\cos\left(\dfrac{n\pi}{w_c}(x-x_o)\right) & x_o\le x\le x_c\\ 0 & \textit{elsewhere}\end{cases}$$

$$\beta_n=\begin{cases}\sqrt{k^2-\left(\dfrac{n\pi}{w_c}\right)^2} & k^2\ge\left(\dfrac{n\pi}{w_c}\right)^2\\ -j\sqrt{\left(\dfrac{n\pi}{w_c}\right)^2-k^2} & k^2<\left(\dfrac{n\pi}{w_c}\right)^2\end{cases}$$

$$y_n=\frac{\omega\varepsilon_0\varepsilon_r}{\beta_n},\ k=k_0\sqrt{\varepsilon_r}$$

Secondly, the fields in region II could be expanded in terms of the Floquet's basis modes as follows

$$E_x^{II}(x,z)=\sum_{m=-\infty}^{\infty}\left(V_m^+e^{-j\xi_m z}+V_m^-e^{j\xi_m z}\right)\Psi_m(x) \tag{6-17a}$$

$$H_y^{II}(x,z)=\sum_{m=-\infty}^{\infty}\left(V_m^+e^{-j\xi_m z}-V_m^-e^{j\xi_m z}\right)Y_m\Psi_m(x) \tag{6-17b}$$

Where

$$\Psi_n(x)=\frac{1}{\sqrt{d}}e^{-jK_{xm}(x-x_o)}$$

$$K_{xm}=\frac{2m\pi+\delta}{d}$$

$$\xi_m = \begin{cases} \sqrt{k^2 - K_{xm}{}^2} & k^2 \geq K_{xm}{}^2 \\ -j\sqrt{K_{xm}{}^2 - k^2} & k^2 < K_{xm}{}^2 \end{cases}$$

$$Y_m = \frac{\omega \varepsilon_0 \varepsilon_r}{\xi_m}$$

On the other hand, the fields in the air (region III) could be expanded as

$$E_x^{III}(x,z) = \sum_{m=-\infty}^{\infty} U_m e^{-j\gamma_m z} \Psi_m(x) \tag{6-18a}$$

$$H_y^{III}(x,z) = \sum_{m=-\infty}^{\infty} U_m e^{-j\gamma_m z} Y_m \Psi_m(x) \tag{6-18b}$$

Where

$$\gamma_m = \begin{cases} \sqrt{k_0{}^2 - K_{xm}{}^2} & k_0{}^2 \geq K_{xm}{}^2 \\ -j\sqrt{K_{xm}{}^2 - k_0{}^2} & k_0{}^2 < K_{xm}{}^2 \end{cases}$$

$$Y_m = \frac{\omega \varepsilon_0}{\gamma_m}$$

We have now two apertures; one on the cavity opening at z=0; "Aperture I" and one at the top substrate $z=h_s$; "Aperture II". Upon matching the electric and magnetic fields at both sides of Aperture I we end up with the following

$$\sum_{n=0}^{\infty} v_n \Phi_n(x) = \sum_{m=-\infty}^{\infty} \left(V_m^+ + V_m^-\right) \Psi_m(x) \tag{6-19a}$$

$$\sum_{n=0}^{\infty} j v_n y_n \Phi_n(x) \cot\left(\beta_n h_c\right) = \sum_{m=-\infty}^{\infty} \left(V_m^+ - V_m^-\right) Y_m \Psi_m(x) \tag{6-19b}$$

Where

$$v_n = v_n \sin\left(\beta_n h_c\right)$$

Taking an inner product of the electric field equation; eq. (6-19a) with $\Psi_p^*(x)$, leads to

$$V_p^+ + V_p^- = \sum_{n=0}^{\infty} v_n C_{np}^* \tag{6-20}$$

Where

$$C_{np}^* = \int_{SA_1} \Phi_n(x).\Psi_p^*(x)dx \ , \ \left\{SA_1 : z = 0, x_0 \leq x \leq x_c\right\}$$

While taking an inner product of the magnetic field equation; eq. (6-19b) with $\Phi_i(x)$, results in

$$v_i = \frac{-j}{y_i \cot(\beta_i h_c)} \sum_{m=-\infty}^{\infty} \left(V_m^+ - V_m^-\right) Y_m C_{im} \tag{6-21}$$

Substituting for v_i in eq. (6-20), we end up with

$$V_p^+ + V_p^- = \sum_{n=0}^{\infty} fy_n \sum_{m=-\infty}^{\infty} \left(V_m^+ - V_m^-\right) Y_m C_{nm} C_{np}^* \tag{6-22}$$

Where

$$fy_n = \frac{-j}{y_n \cot(\beta_n h_c)}$$

Equation (6-22) could be reduced to the matrix form

$$(\mathbf{I}+\mathbf{B})\mathbf{V}^+ = -(\mathbf{I}-\mathbf{B})\mathbf{V}^- \tag{6-23}$$

Where

$$\mathbf{B} = \mathbf{fy}.\mathbf{C}.\mathbf{Y}.\mathbf{C}^*,$$

I is an identity matrix

Then could be reduced to

$$\mathbf{V}^- = \mathbf{S}.\mathbf{V}^+ \tag{6-24}$$

Where

$$\mathbf{S} = -(\mathbf{I}-\mathbf{B})^{-1}(\mathbf{I}+\mathbf{B})$$

Then upon matching the electric and magnetic fields at both sides of Aperture II ($z=h_s$), we end up with the following

$$E_b(x) = \sum_{m=-\infty}^{\infty} \left(V_m^+ e^{-j\xi_m h_s} + V_m^- e^{j\xi_m h_s}\right) \Psi_m(x) = \sum_{m=-\infty}^{\infty} U_m \Psi_m(x) \tag{6-25a}$$

$$J_s(x) = \sum_{m=-\infty}^{\infty} \left(Y_m U_m - Y_m \left(V_m^+ e^{-j\xi_m h_s} - V_m^- e^{j\xi_m h_s}\right)\right) \Psi_m(x) \tag{6-25b}$$

Where $E_b(x)$ is the field on Aperture II that could be expanded in terms of left and right aperture basis

$$E_b^-(x,0^-) = E_b^+(x,0^+) = E_l + E_r \tag{6-26}$$

Where

$$E_l = \sum_{i=0}^{\infty} a_i \Theta_i(x)$$

$$E_r = \sum_{n=0}^{\infty} b_n \Theta_i(x)$$

and

Basis on left aperture: $\Theta_n(x) = \begin{cases} \dfrac{\mathrm{Cos}\left(\dfrac{2\mathrm{n}\pi}{\mathrm{t}} \cdot \mathrm{x}\right)}{\sqrt{1-\left(\dfrac{2\mathrm{x}}{\mathrm{t}}\right)^2}} & 0 \le x \le t/2 \\ 0 & \textit{elsewhere} \end{cases}$

Basis on right aperture: $\Theta_n(x) = \begin{cases} \dfrac{\mathrm{Cos}\left(\dfrac{2\mathrm{n}\pi}{\mathrm{t}} \cdot (d - \mathrm{x})\right)}{\sqrt{1-\left(\dfrac{2(\mathrm{d}-\mathrm{x})}{\mathrm{t}}\right)^2}} & t/2 + a \le x \le d \\ 0 & \textit{elsewhere} \end{cases}$

Resulting in

$$\sum_{i=0}^{\infty} a_i \Theta_i(x) + \sum_{n=0}^{\infty} b_n \Theta_n(x) = \sum_{m=-\infty}^{\infty} \left(V_m^{+} e^{-j\xi_m h} + V_m^{-} e^{j\xi_m h}\right) \Psi_m(x) = \sum_{m=-\infty}^{\infty} U_m \Psi_m(x) \qquad (6\text{-}27)$$

Taking an inner product to eq. (6-27) with $\Psi_p^*(x)$ leads us to the following

$$U_p = \left(V_p^{+} e^{-j\xi_p h} + V_p^{-} e^{j\xi_p h}\right) = \sum_{i=0}^{\infty} a_i f_{ip}^{*} + \sum_{n=0}^{\infty} b_n g_{np}^{*} \qquad (6\text{-}28)$$

Where

$$f_{ip}^{*} = \int_{SL} \Theta_i(x).\Psi_p^*(x)dx$$

$$g_{np}^{*} = \int_{SR} \Theta_n(x).\Psi_p^*(x)dx$$

$\{SL : z = h_s, 0 \le x \le t/2\}$, and $\{SR : z = h_s, a + t/2 \le x \le d\}$

Equation (6-28) could be reduced to the matrix form

$$\mathbf{U} = \mathbf{f}^{*}\mathbf{a} + \mathbf{g}^{*}\mathbf{b} \qquad (6\text{-}29)$$

Then V^+ could be calculated as

$$\mathbf{V}^{+} = \mathbf{P}^{-1}\mathbf{U} \qquad (6\text{-}30)$$

Where

$$\mathbf{P} = \mathbf{e}^{-j\xi h_s} + \mathbf{S}.\mathbf{e}^{j\xi h_s}$$

Testing eq. (6-25b) by $\Theta_q(x)$ results in

$$\vartheta_q = \sum_{m=-\infty}^{\infty} \left(Y_m U_m - Y_m \left(V_m^+ e^{-j\xi_m h_s} - V_m^- e^{j\xi_m h_s} \right) \right) f_{qm} \tag{6-31}$$

Where

$$\vartheta_q = \int_{SL} J_s(x).\Theta_q(x) dx$$

Which could be written in a matrix form as

$$\mathbf{J} = \mathbf{FHF}^* \mathbf{a} + \mathbf{FHG}^* \mathbf{b} \tag{6-31a}$$

Where

$$\mathbf{H} = diag\left(Y\right) - diag\left(Y\right).\mathbf{Q}.\mathbf{P}^{-1}$$

and

$$\mathbf{Q} = \mathbf{e}^{-j\xi h_s} + \mathbf{S}.\mathbf{e}^{j\xi h_s}$$

Similarly, by taking inner product of eq. (6-25b) by $\Theta_q(x)$, we end up with a second matrix equation

$$\mathbf{J} = \mathbf{GHF}^* \mathbf{a} + \mathbf{GHG}^* \mathbf{b} \tag{6-31b}$$

Where

$$\vartheta_q = \int_{SR} J_s(x).\Theta_q(x) dx$$

By solving equations (6-31a) and (6-31b), we can find the coefficient vectors *a* and *b*, then we can find the voltage coefficients $\mathbf{U}$, $\mathbf{V}^+$, $\mathbf{V}^-$ and *v* using eq. (6-29, 30, 24 and 21), respectively.

6.4.3 **Active Impedance**

The active impedance of the cavity-backed patch phased array could be calculated following again the definition of Liu in [5]

$$Z_a = \int_{-h_c}^{h_s} \frac{E_z dz}{K_0 d_p} \tag{6-32}$$

Where d_p is the probe spacing in the uniform direction which should not exceed $\lambda_0/2$, a spacing of $\lambda_0/3$ (at midband) was used. Applying the active impedance integral results in

$$Z_a = -\frac{v_3^+ + v_3^-}{I_0} + \frac{1}{I_0}\left[\sum_{n=0}^{\infty} c_{g_n} v_n + \sum_{m=-\infty}^{\infty} \left(c_{fl_m} V_m^+ - c_{fl_m} V_m^- \right) \right] \tag{6-33}$$

Where the first term corresponds to the integral of the electric field calculated from the feed problem in section 6.3.1 with v_3^+, and v_3^- being the incident and reflected voltages on the transmission line at node 3, while the second term corresponds to integral of the electric field in region I of the radiation problem in section 6.3.2 with v_n being the voltage coefficients of the waveguide modes. Finally, the third term corresponds to integral of the electric field in region II of the radiation problem with V_m^+ and V_m^- being the voltage incident and reflected coefficients of the Floquet's modes in the dielectric region, while

$$c_{g_n} = \sqrt{\frac{2}{w_c}} \frac{n\pi}{w_c \beta_n^2} \cdot \sin\left(\frac{n\pi}{w_c}(x' - x_0)\right)$$

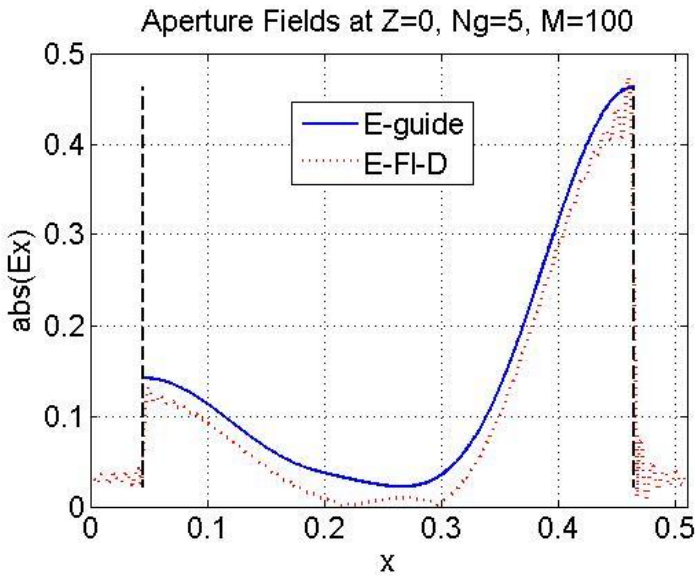
$$c_{fl_m} = \frac{2}{\sqrt{d}} \frac{K_{xm}}{\xi_m^2} e^{-jK_{xm}x'} \cdot \sin\left(\xi_m \frac{h}{2}\right) e^{-j\xi_m \frac{h}{2}}$$

$$c_{fl_m} = \frac{2}{\sqrt{d}} \frac{K_{xm}}{\xi_m^2} e^{-jK_{xm}x'} \cdot \sin\left(\xi_m \frac{h}{2}\right) e^{j\xi_m \frac{h}{2}}$$

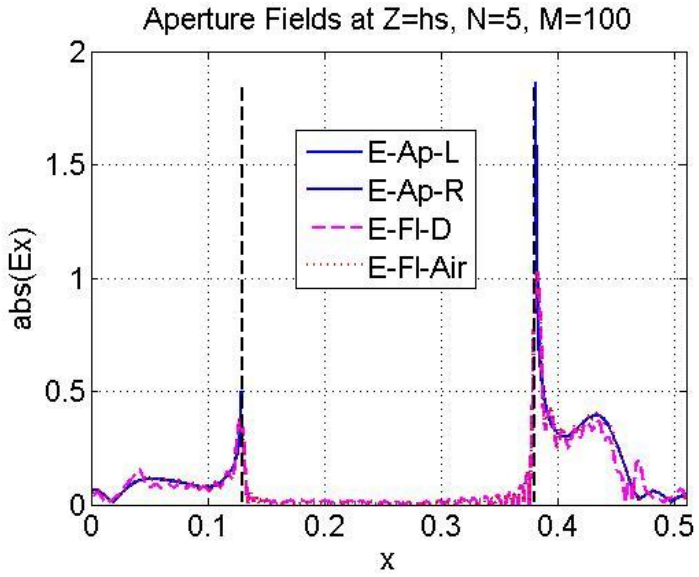
The two series of the active impedance expression will be truncated to Ng, and M terms respectively.

6.4.4 **Numerical Results**

Let's consider a case study where $\varepsilon_{rs}=\varepsilon_{rc}=2.2$, $h_s=0.01\lambda_0$, $h_c=0.12\lambda_0$, $d=0.51\lambda_0$, $a=0.25\lambda_0$, $x_f=0$, and $W_c=0.42\lambda_0$. Figure **6.15** shows the aperture electric fields calculated from the radiation problem of the cavity-backed patch phased array on both apertures (i.e Aperture I; z=0 and Aperture II; $z=h_s$). A good field matching is obtained on Aperture I as shown in Figure **6.15**(a), where the blue line depicts the electric field calculated from the waveguide side (Ng is the number of guide basis modes; Ng=5) while the dotted red line is the electric field calculated from the Floquet's sum in the dielectric (M is the number of Floquet basis modes; based on our previous experience with the microstrip phased array, we have used M=20Ng=100). Similar field matching exists also on the Aperture II as shown in Figure **6.15**(b), where the blue line depicts the electric field calculated from the basis expansion on the aperture (N is the number of basis modes; N=Ng=5), and the dashed magenta is electric field calculated from the Floquet's sum in the dielectric. Both Floquet's sums in the dielectric and air were truncated to M (M=20N=100).



(a)



(b)

Figure 6.15 Aperture fields calculated from the radiation problem of the cavity-backed patch phased array (case of two substrates) in case of $\varepsilon_{rs}=\varepsilon_{rc}=2.2$, $h_s=0.01\lambda_0$, $h_c=0.12\lambda_0$, $d=0.51\lambda_0$, $a=0.25\lambda_0$, $x_f=0$, and $W_c=0.42\lambda_0$. (a) Fields on Aperture I (i.e. z=0), Ng=5, and M=100. (b) Fields on Aperture II (i.e. $z=h_s$), N=5, and M=100.

The E-plane scan performance of the cavity-backed patch phased array for the same case study ($\varepsilon_{rs}=\varepsilon_{rc}=2.2$, $h_s=0.01\lambda_0$, $h_c=0.12\lambda_0$, $d=0.51\lambda_0$, $a=0.25\lambda_0$, $x_f=0$, and $W_c=0.42\lambda_0$) is shown in Figure 6.16 compared to that of the corresponding microstrip phased array. The array was broadside matched to 50 Ω like [5] based on $Z_{a-matched}=\left(Z_a+Z_B^{*}\right).50/\left(2.real\left(Z_B\right)\right)$ where Z_B is the active impedance at broadside.

Clearly, the cavity-backed patch phased array exhibits wider scan performance rather than that of the microstrip phased array and doesn't suffer from the weak scan blindness appears in the scan range of the microstrip array at 59°. Despite that we expect the scan range of the 3-D phased array to be not quantitatively similar to the one obtained using our 2-D analysis, the obtained numerical results qualitatively demonstrates the potential of the cavity in increasing the limited scan range of the microstrip phased arrays alleviating the problem of scan blindness that appear in relatively thick substrate microstrip phased arrays.

It worth noting also the anomaly in the calculated scan performance at 20°, which we attribute to the inherent singularity appeared because of applying the equivalence theorem here, where we are solving for coupled integral equations on the two apertures. It is very difficult to get rid of this anomaly in the numerical solution; however the actual array performance won't have such an anomaly.

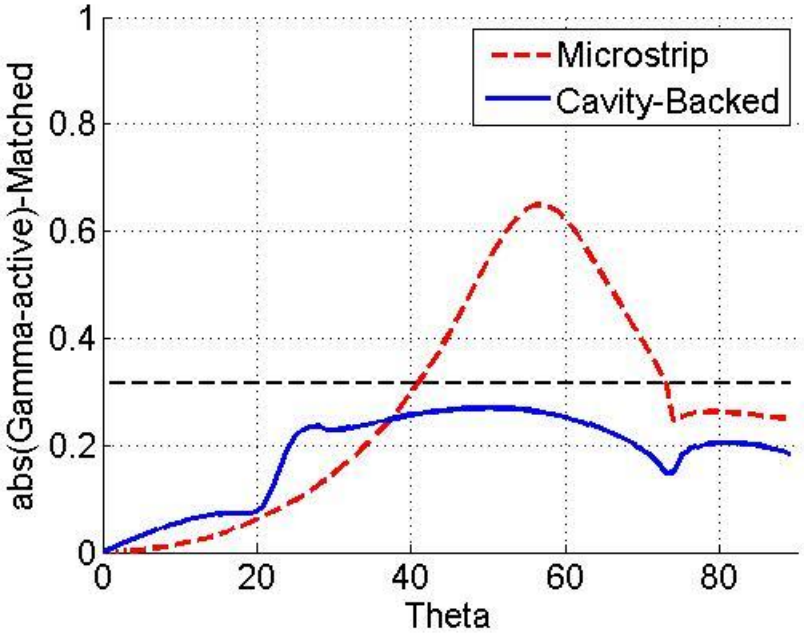
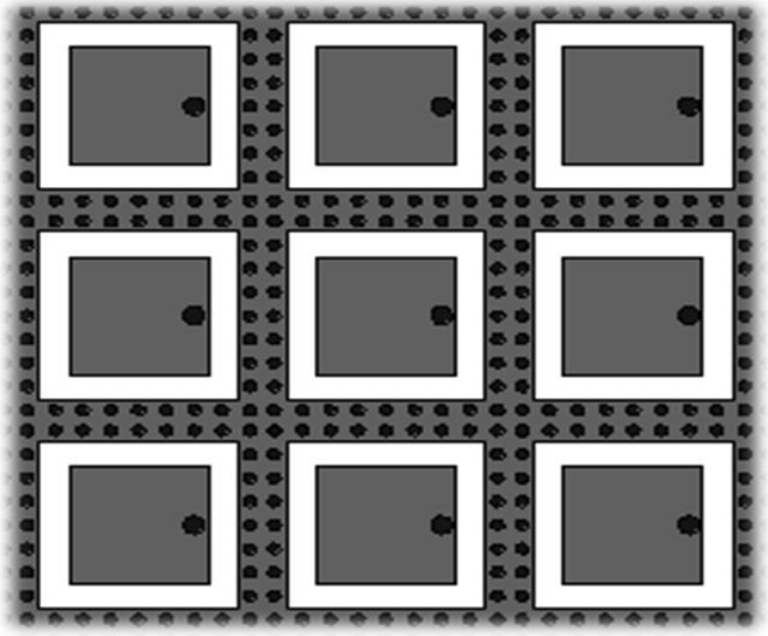


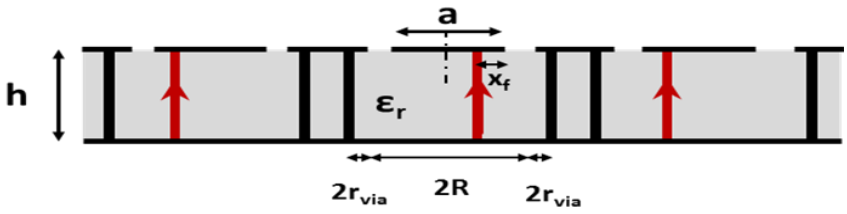
Figure 6.16 E-plane scan performance of the cavity-backed patch phased array (case of two substrates) compared to that of the microstrip phased array in case of $\varepsilon_{rs}=\varepsilon_{rc}=2.2$, $h_s=0.01\lambda_0$, $h_c=0.12\lambda_0$, $d=0.51\lambda_0$, $a=0.25\lambda_0$, $x_f=0$, and $W_c=0.42\lambda_0$.

6.5 Analysis of Probe-Fed Cavity-Backed Patch Phased Array (Case of a Single Substrate)

Now, let's consider the case where the patch is right away on the cavity aperture as shown in Figure **6.17**. Again, in order to simplify the SIW structure, the SIW walls will be replaced by continuous metal walls of equivalent side length W_c, as shown in Figure 6.18. Then following the same theme of the previous microstirp and cavity-backed (two substrates) phased array cases, the problem could be analyzed using the equivalence principle where it could be divided into two separate problems; feed problem and radiation problem, as shown in Figure 6.18



(a)



(b)

Figure 6.17 Proposed array of SIW cavity-backed microstrip patches (case of a single substrate).

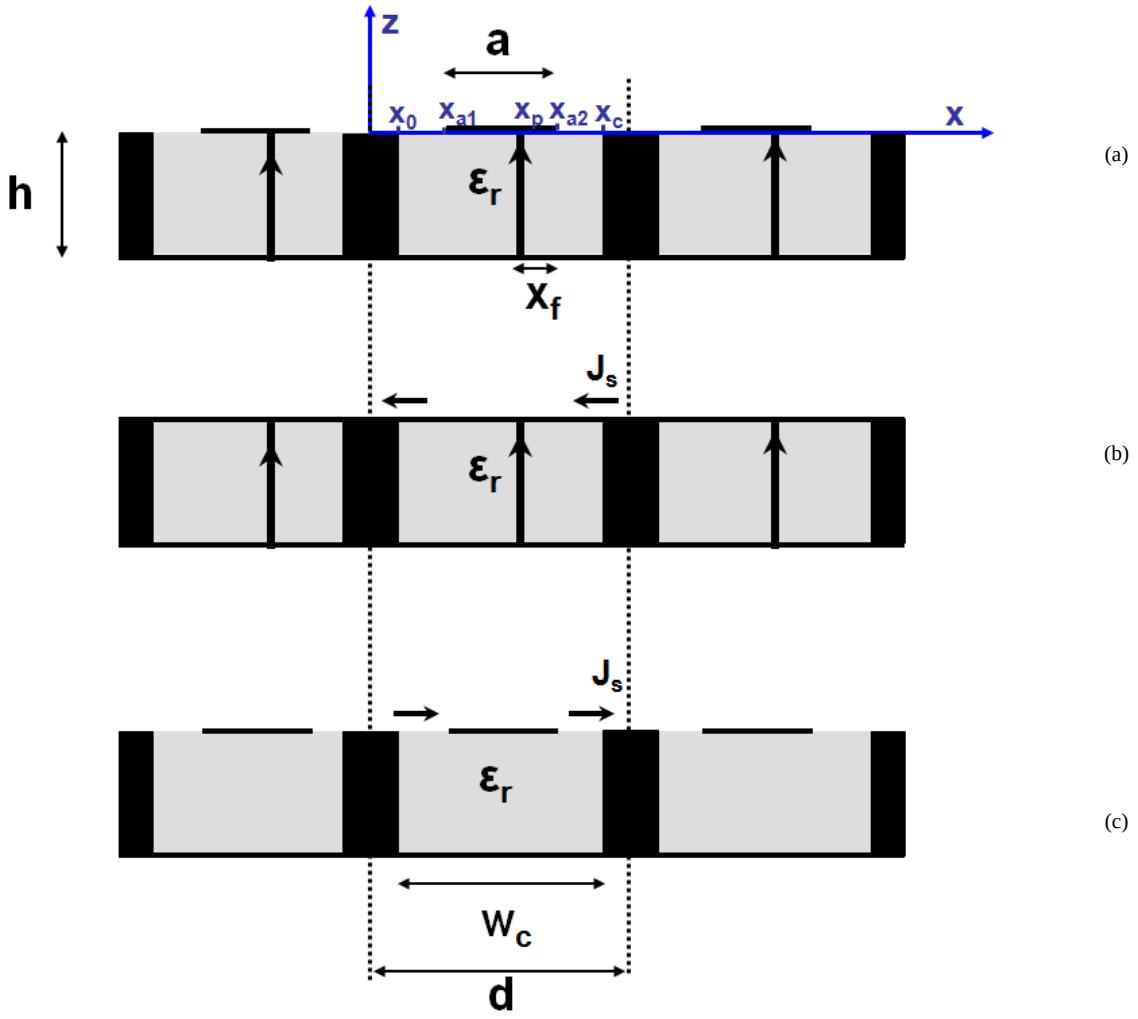


Figure 6.18 SIW phased array of cavity-backed patches (case of a single substrate) (a) Simplified 2-D problem. (b) Equivalent feed problem. (c) Equivalent radiation problem.

6.5.1 **Feed Problem**

The feed problem can be modeled as a closed rectangular waveguide excited by a sheet current excitation, as shown in Figure 6.18(b). Upon using the dyadic Green's function of the rectangular waveguide [97] , the surface current on the top waveguide wall could be calculated as

$$J_{sx} = H_y\big|_{z=0}$$

$$H_y = -\frac{1}{\mu}\left(\frac{\partial A_z}{\partial x} - \frac{\partial A_x}{\partial z}\right)$$

$$A = \int G_e\left(r \mid r'\right).J_f\left(r'\right)dv'$$

Where $G_e\left(r \mid r'\right)$ is the electrical dyadic Green's function in rectangular waveguide.

$$J_f = f\left(z'\right)\delta(x'-x_p)a_z$$

Which leads to

$$J_{sx} = -\frac{e^{-j\delta}}{4\mu w_c}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{\mathrm{I_m}\,\varepsilon_{0n}\varepsilon_{0m}}{\Gamma_{nm}}\left(\frac{n\pi}{w_c}\right)(-1)^m \sin\left(\left(\frac{n\pi}{w_c}\right)\left(x_p - x_o\right)\right)\cos\left(\left(\frac{n\pi}{w_c}\right)\left(x - x_o\right)\right) \qquad (6\text{-}34)$$

Where

$$\Gamma_{nm} = -k^2 + \left(\frac{n\pi}{w_c}\right)^2 + \left(\frac{m\pi}{h}\right)^2$$

$$\mathrm{I_m} = \frac{k^2}{j\omega\sum_{n=0}^{\infty}\frac{\varepsilon_{0n}h}{4w_c\Gamma_{nm}}\left(\left(\frac{n\pi}{w_c}\right)^2 - \Gamma_{nm}^2\right)\sin\left(\left(\frac{n\pi}{w_c}\right)\left(x_p - x_o\right)\right)^2}$$

$$\varepsilon_{0m} = \begin{cases} 1 & m = 0 \\ 2 & m \neq 0 \end{cases}$$

6.5.2 **Radiation Problem**

Regarding the radiation problem unit cell, shown in Figure **6.19**, the numerical solution of the boundary value problem could be divided again into two regions. In each region the field could be expanded in terms of the corresponding basis modes of the region. First the fields in region I could be expanded in terms of the waveguide basis modes as follows

$$E_x^I(x,z) = \sum_{n=0}^{\infty} v_n \Phi_n(x)\sin\left(\beta_n(z+h)\right) \qquad (6\text{-}35a)$$

$$H_y^I(x,z) = \sum_{n=0}^{\infty} jv_n y_n \Phi_n(x)\cos\left(\beta_n(z+h)\right) \qquad (6\text{-}35b)$$

Where

$$\Phi_n(x) = \begin{cases} \sqrt{\frac{2}{w_c}}\cos\left(\frac{n\pi}{w_c}(x - x_o)\right) & x_o \le x \le x_c \\ 0 & \textit{elsewhere} \end{cases}$$

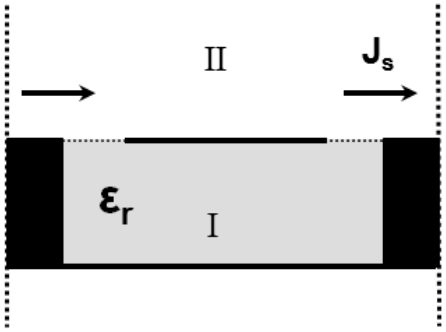


Figure 6.19 Radiation problem unit cell of the cavity-backed patch phased array (case of a single substrate).

and

$$\beta_n = \begin{cases} \sqrt{k^2 - \left(\dfrac{n\pi}{w_c}\right)^2} & k^2 \geq \left(\dfrac{n\pi}{w_c}\right)^2 \\ -j\sqrt{\left(\dfrac{n\pi}{w_c}\right)^2 - k^2} & k^2 < \left(\dfrac{n\pi}{w_c}\right)^2 \end{cases}$$

$$y_n = \frac{\omega\varepsilon_0\varepsilon_r}{\beta_n},\ k = k_0\sqrt{\varepsilon_r}$$

On the other hand, the fields in the air, region II, could be expanded as

$$E_x^{II}(x,z) = \sum_{m=-\infty}^{\infty} V_m e^{-j\gamma_m z}\Psi_m(x) \tag{6-36a}$$

$$H_y^{II}(x,z) = \sum_{m=-\infty}^{\infty} V_m e^{-j\gamma_m z} Y_m \Psi_m(x) \tag{6-36b}$$

Where

$$\gamma_m = \begin{cases} \sqrt{k_0^2 - K_{xm}^2} & k_0^2 \geq K_{xm}^2 \\ -j\sqrt{K_{xm}^2 - k_0^2} & k_0^2 < K_{xm}^2 \end{cases}$$

$$Y_m = \frac{\omega\varepsilon_0}{\gamma_m}$$

In this case, we have a split aperture on the cavity opening at z=0. Upon matching the electric and magnetic fields on both sides of this aperture, we end up with the following

$$E_{aperture}(x)=\sum_{n=0}^{\infty}v_n\Phi_n(x)=\sum_{m=-\infty}^{\infty}V_m\Psi_m(x) \tag{6-37a}$$

$$J_s(x)=\sum_{m=-\infty}^{\infty}V_mY_m\Psi_m(x)-\sum_{n=0}^{\infty}jv_ny_n\Phi_n(x)\cot\left(\beta_n h_c\right) \tag{6-37b}$$

Where

$$v_n=v_n\sin\left(\beta_n h_c\right)$$

and $E_{aperture}(x)$ is the field on the cavity aperture that could be expanded in terms of left and right aperture basis modes

$$E_{aperture}(x)=E_l+E_r \tag{6-38}$$

Where

$$E_l=\sum_{i=0}^{\infty}a_i\Omega_i(x)$$

$$E_r=\sum_{n=0}^{\infty}b_n\Omega_i(x)$$

and

$$\Omega_n(x)=\begin{cases}\dfrac{\cos\left(\dfrac{2n\pi}{t}\cdot\left(x-x_o\right)\right)}{\sqrt{1-\left(\dfrac{2\left(x-x_o\right)}{t}\right)^2}} & x_o\le x\le x_{a1}\\ 0 & elsewhere\end{cases}$$

$$\Omega_n(x)=\begin{cases}\dfrac{\cos\left(\dfrac{2n\pi}{t}\cdot\left(x_c-x\right)\right)}{\sqrt{1-\left(\dfrac{2\left(x_c-x\right)}{t}\right)^2}} & x_{a2}\le x\le x_c\\ 0 & elsewhere\end{cases}$$

So that

$$\sum_{i=0}^{\infty}a_i\Omega_i(x)+\sum_{n=0}^{\infty}b_n\Omega_n(x)=\sum_{n=0}^{\infty}v_n\Phi_n(x)=\sum_{m=-\infty}^{\infty}V_m\Psi_m(x) \tag{6-39}$$

Taking an inner product of eq. (6-39) with $\Psi_p^*(x)$ leads us to the following

$$V_p = \sum_{n=0}^{\infty} v_n C_{np}^* = \sum_{i=0}^{\infty} a_i f_{ip}^* + \sum_{n=0}^{\infty} b_n f_{np}^* \tag{6-40}$$

Where

$$f_{ip}^* = \int_{SL} \Omega_i(x).\Psi_p^*(x)dx$$

$$f_{np}^* = \int_{SR} \Omega_n(x).\Psi_p^*(x)dx$$

Equation (6-40) could be written in a matrix form as

$$\mathbf{V} = \mathbf{f}^*\mathbf{a} + \tilde{\mathbf{f}}^*\mathbf{b} \tag{6-41a}$$

and

$$\mathbf{v} = \mathbf{C}^{*-1}\mathbf{V} \tag{6-41b}$$

Testing the magnetic field equation; eq. (6-37b) by $\Omega_q(x)$ results in

$$\vartheta_q = \sum_{m=-\infty}^{\infty} Y_m V_m f_{qm} - \sum_{n=0}^{\infty} y_n v_n g_{qn} \tag{6-42}$$

Where

$$\vartheta_q = \int_{SL} J_s(x).\Omega_q(x)dx$$

$$g_{ip} = \int_{SL} \Omega_i(x).\Phi_p(x)dx$$

$$g_{np} = \int_{SR} \Omega_n(x).\Phi_p(x)dx$$

$$y_n = jy_n \cot(\beta_n h_c)$$

Upon substituting for $\mathbf{v} = \mathbf{C}^{*-1}\mathbf{V}$ in eq. (6-42), it could be written in a matrix form as

$$\mathbf{J} = \mathbf{F}\cdot\mathbf{diag(Y)}\mathbf{F}^*\mathbf{a} + \mathbf{F}\cdot\mathbf{diag(Y)}\mathbf{F}^*\mathbf{b} - \mathbf{G}\cdot\mathbf{diag(y)}\mathbf{C}^{*-1}\mathbf{F}^*\mathbf{a} - \mathbf{G}\cdot\mathbf{diag(y)}\mathbf{C}^{*-1}\mathbf{F}^*\mathbf{b} \tag{6-43a}$$

Similarly, by testing eq. (6-37b) with $\Omega_q(x)$, we end up with a second matrix equation

$$\mathbf{J} = \mathbf{F}\cdot\mathbf{diag(Y)}\mathbf{F}^*\mathbf{a} + \mathbf{F}\cdot\mathbf{diag(Y)}\mathbf{F}^*\mathbf{b} - \mathbf{G}\cdot\mathbf{diag(y)}\mathbf{C}^{*-1}\mathbf{F}^*\mathbf{a} - \mathbf{G}\cdot\mathbf{diag(y)}\mathbf{C}^{*-1}\mathbf{F}^*\mathbf{b} \tag{6-43b}$$

Where

$$\vartheta_q = \int_{SR} J_s(x).\Omega_q(x)dx$$

Upon solving eq. (6-43a) and (6-43b), we can find the coefficient vectors *a* and *b*, then we can find the voltage coefficients $\mathbf{V}$ and $\mathbf{v}$ using eq. (6-41a) and (6-41b), respectively.

6.5.3 **Active Impedance**

The active impedance of the probe-fed microstrip phased array could be calculated following again the definition of Liu in [5]

$$Z_a = \int_{-h}^{0} \frac{E_z dz}{K_0 d_p} \tag{6-44}$$

Where d_p is the probe spacing in the uniform direction which should not exceed $\lambda_0/2$, a spacing of $\lambda_0/3$ (at midband) was used. Applying the active impedance integral results in

$$Z_a = \frac{j\omega h e^{-j\delta}}{4w_c k^2} \sum_{n=0}^{\infty} \frac{\varepsilon_{0n}}{\Gamma_{n0}} \left(\left(\frac{n\pi}{w_c} \right)^2 - \Gamma_{n0}^2 \right) \sin^2 \left(\frac{n\pi}{w_c} \left(x_p - x_0 \right) \right) -$$
$$\frac{1}{I_0 \omega \varepsilon} \sqrt{\frac{2}{w_c}} \sum_{i=0}^{\infty} \frac{n\pi}{w_c} \frac{y_n}{\beta_n} \sin \left(\frac{n\pi}{w_c} \left(x_p - x_0 \right) \right) v_n \tag{6-45}$$

Where the first part in the active impedance expression corresponds to the integral of the electric field calculated from the feed problem; section 6.4.1, while the second part corresponds to the integral of the electric field calculated from the radiation problem; section 6.4.2 with v_n being the voltage coefficients of the waveguide modes in region I. In the numerical solution, the feed-problem series (first term) of the active impedance expression will be truncated to N_f terms, while the waveguide modes series (second term) will be truncated to Ng terms.

6.5.4 **Numerical Results**

Let's consider the case of cavity-backed patch phased array (single substrate) with the following parameters; $d=0.5\lambda_0$, $a=0.27\lambda_0$, $x_f=a/15$, $\varepsilon_r=2.2$, $h_c=0.06\lambda_0$, and $W_c=0.4\lambda_0$.

Using the developed 2-D numerical code, the electric fields on the aperture have been calculated, as shown in Figure **6.20**. A good field matching is obtained on the aperture, where the blue line depicts the electric field calculated from the basis expansion (N is the number of basis modes; here N=3), while the

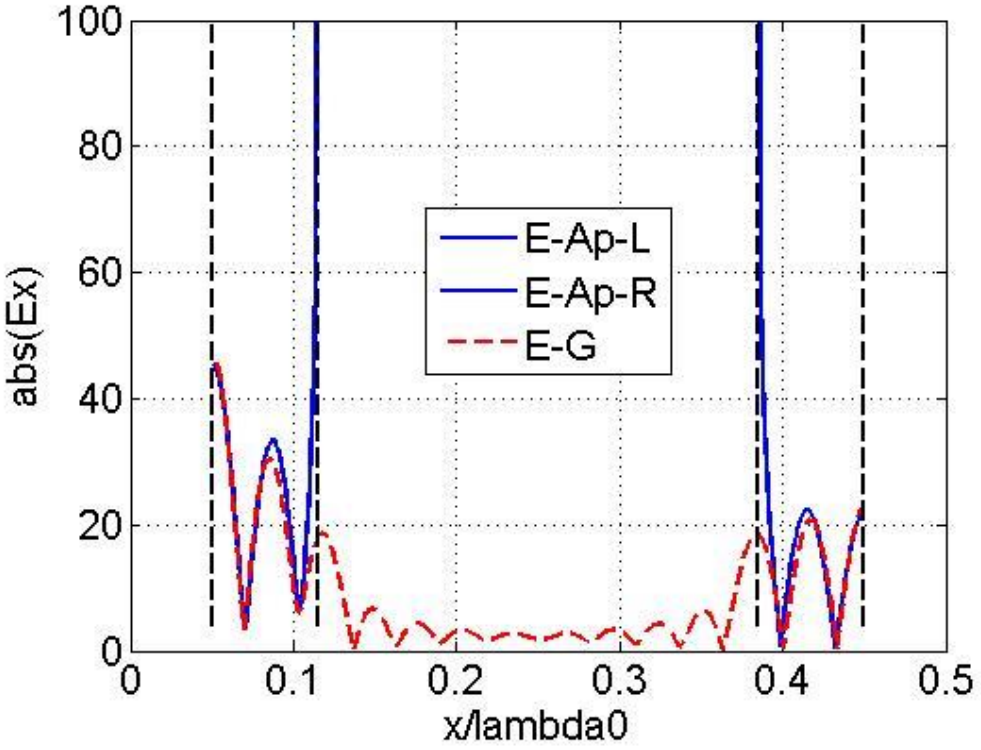


Figure 6.20 Aperture fields of the cavity-backed phased array (case of a single substrate) calculated in case of $d=0.5\lambda_0$, a=0.27λ0, $x_f=a/15$, $\varepsilon_r=2.2$, $h=0.10\lambda_0$, and $W_c=0.4\lambda_0$ (for $N_f=5$, Ng=16).

dashed red line is the electric field calculated from the waveguide modes sum (Ng is the number of waveguide basis modes; here Ng=16).

Now, let's consider the E-plane scan performance of the cavity-backed patch array for the case of $d=0.5\lambda_0$, a=0.27λ0, $x_f=a/15$, $\varepsilon_r=2.2$, $W_c=0.4\lambda_0$, and for various substrate thicknesses specifically; $h=0.06\lambda_0$, $h=0.08\lambda_0$, and $h=0.10\lambda_0$. Figure **6.21**-23 shows the numerically calculated E-plane scan range of the cavity-backed patch phased array compared to that calculated for the corresponding microstrip array. The active reflection coefficient is matched with respect to the broadside impedance Z_B [47]

$$R_{active-matched} = \frac{Z_a - Z_B}{Z_a + Z_B^*} \tag{6-46}$$

Unlike the microstrip arrays, the E-plane scan performance of the cavity-backed patch phased array gets wider upon increasing the substrate thickness. For instance, the scan range of the cavity-backed patch array in case of $h=0.06\lambda_0$ is about 58º compared to 49º for the microstrip array, as shown in Figure **6.21**. The scan range of the cavity-backed patch array increases to 65º upon increasing the substrate thickness to $0.08\lambda_0$, while it decreases to 44º in case of microstrip as shown in Figure **6.22**. Increasing the substrate

thickness even further to $0.10\lambda_0$ widens the scan range of the cavity-backed array to 73º, while it narrows down the scan range of the microstrip array to 40º as shown in Figure **6.23**.

Clearly, that shows the potential of using the cavities to impede the surface waves and so widens the scan range solving the limited scan range problem of the microstrip phased arrays. Despite again that we expect the scan performance of the 3-D phased array (that will be investigated in next chapter) to be not quantitatively similar to the one obtained using our 2-D analysis, the obtained numerical results qualitatively demonstrates the potential of the cavity in increasing the limited scan range of the microstrip phased arrays alleviating the problem of scan blindness that appear in relatively thick substrate microstrip phased arrays.

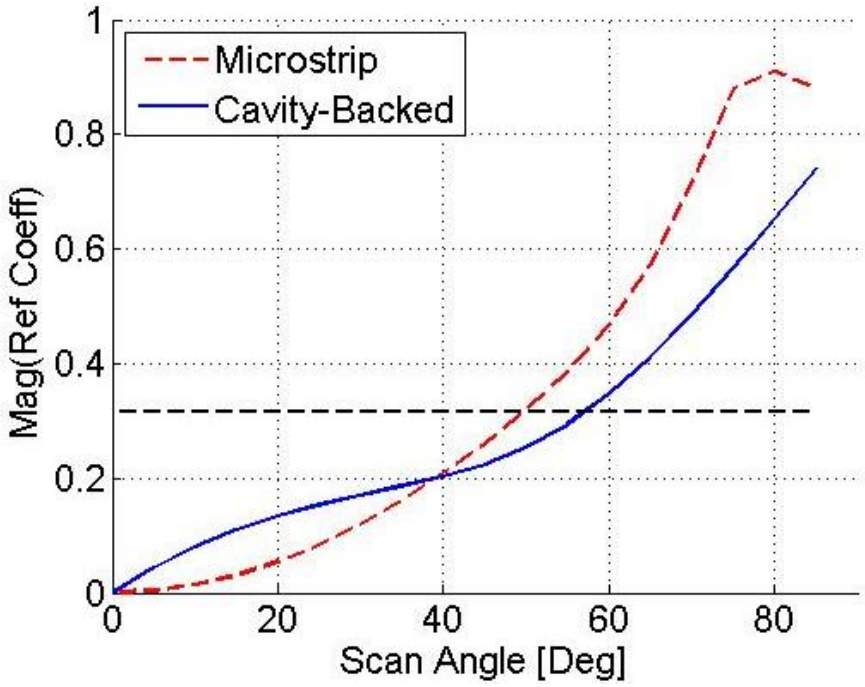


Figure 6.21 E-plane scan performance of the cavity-backed patch phased array (case of a single substrate) compared to that of the microstrip phased array assuming $d=0.5\lambda_0$, $a=0.27\lambda 0$, $x_f=a/15$, $\varepsilon_r=2.2$, $h=0.06\lambda_0$, and $W_c=0.4\lambda_0$.

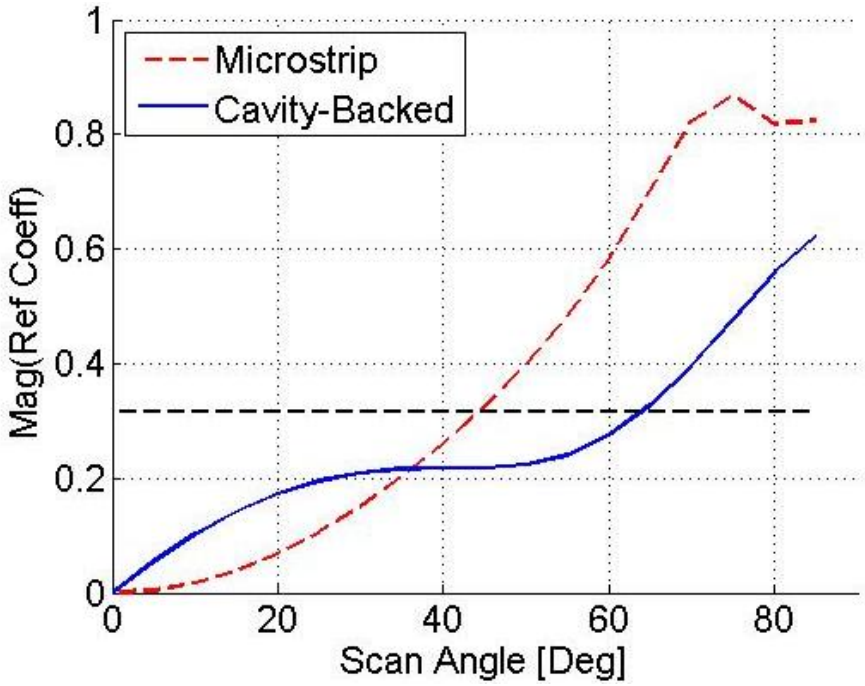


Figure 6.22 E-plane scan performance of the cavity-backed patch phased array (case of a single substrate) compared to that of the microstrip phased array assuming d=0.5λ_0, a=0.27λ0, x_f=a/15, ε_r=2.2, h=0.08λ_0, and W_c=0.4λ_0.

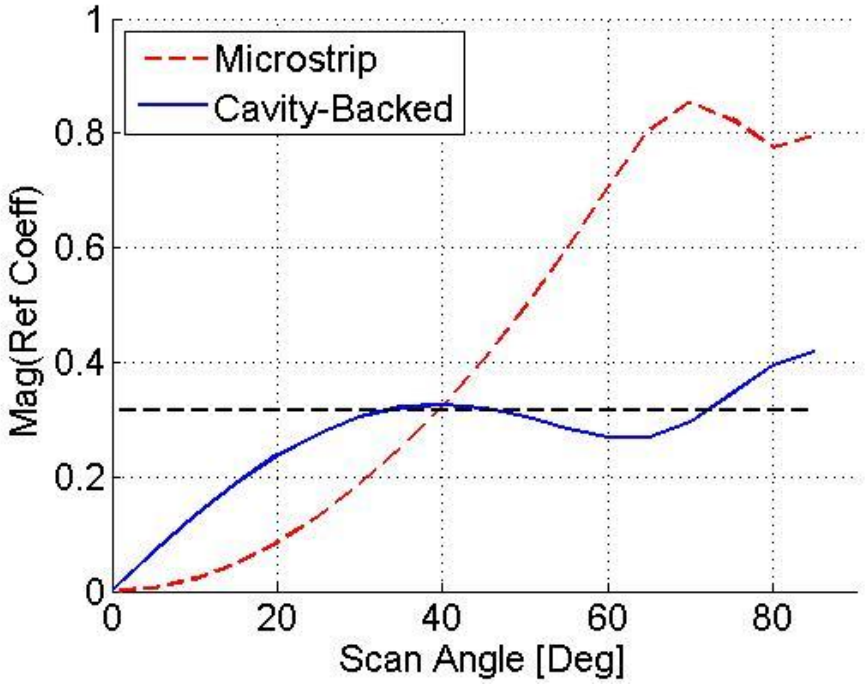


Figure 6.23 E-plane scan performance of the cavity-backed patch phased array (case of a single substrate) compared to that of the microstrip phased array assuming d=0.5λ_0, a=0.27λ0, x_f=a/15, ε_r=2.2, h=0.10λ_0, and W_c=0.4λ_0.

6.6 Conclusion

A simplified 2-D analysis to both the microstrip and cavity-backed patch phased arrays has been carried out to initially investigate the scan range in each case, and demonstrate the potential of cavity-backed patches in enhancing the limited scan range of the conventional microstrip phased arrays. Using the 2-D analysis, the E-plane scan performance of the cavity-backed patch array has been calculated for two distinctive cases; in the first case the structure is comprised of two substrates, where the patch is printed on a separate substrate above another substrate, where the cavity is implemented. The other case is comprised of just one substrate, where the patch is printed on the top conductor of the cavity substrate. The numerically calculated scan performances qualitatively indicates the potential of using the cavities to impede the surface waves, thus enhancing the limited scan range exhibited by the conventional microstrip phased arrays. Moving to 3D analysis would imply more involved formulation and complicated numerical analysis, which is not necessary given the capabilities of nowadays EM simulation tools. Subsequently, further studies of the scan performance in both E- and H-planes will be demonstrated in Chapter 7 using, however commercial EM simulation tool (CST microwave studio).

Chapter 7 Wide-Scan Angle Wide-Band SIW Cavity-Backed Patches Phased Arrays

In this chapter, SIW cavity-backed patches are employed to realize wide-scan wide-band microstrip patch phased arrays. The proposed phased arrays are composed of microstrip patches backed by the substrate-integrated cavities and are probe-fed by SMAs. The scan performance of the proposed phased arrays is further investigated varying both the substrate thickness and dielectric constant. Simple design guides lines for the cavity, patch, and substrate selection are then presented. For demonstration, a 7x7 phased array of the proposed SIW cavity-backed patch structure has been fabricated and its measured results agreed well with theoretical predictions and indicated a relatively wide-scan performance, when compared to the corresponding microstrip patch phased array without cavities.

7.1 Microstrip Antennas Scan Limitation

Microstrip patch phased arrays suffer from the serious problem of scan blindness where most of the electromagnetic energy reflected back to the feed source at certain scan angle\s. The scan blindness problem arises basically from the mutual coupling interaction between the different cells of the phased array, due to surface wave propagation, that destructively sum at certain scan angle\s [98].

The microstrip phased array as a planar structure is very susceptible to surface wave propagation and so to scan blindness as have been demonstrated previously in the literature by many authors [5-11, 43-44, 47, 67, 96, 99-100]. The limited scan problem gets even worse upon increasing the thickness of the microstrip substrate [5, 8], as the more rapid variation in the active impedance versus scan angle can severely limit scan range. However, thick substrates are usually needed in order to increase the limited bandwidth of microstrip patches.

Various techniques have been proposed in that perspective in order to eliminate the scan blindness and maintain both wide impedance bandwidth and wide scan range of operation in microstrip phased arrays. The proposed techniques range from substrate modifications [38], using electromagnetic bandgap (EBG) or periodic bandgap (PBG) structures [39-42], employing shorting posts [43-44], using defected ground structures (DGS) [45-46], to adding cavities underneath the radiating elements [10, 47].

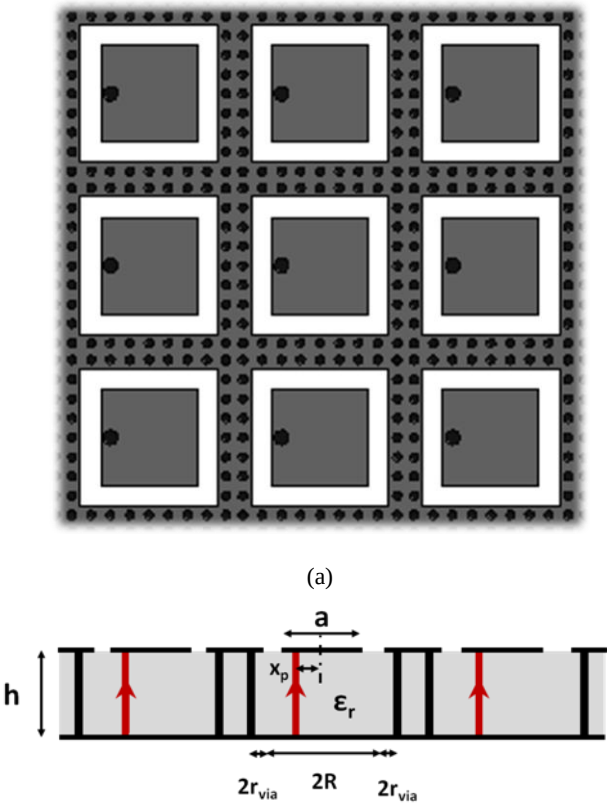
In this chapter, we are investigating the usage of SIW cavity-backed patches instead of the conventional metalized cavities like [47] in phased arrays, targeting to demonstrate its potential in

improving the scan performance of microstrip phased array. Moreover, the implementation of SIW instead of solid cavity metal walls has the benefits of reducing the weight and lowering the cost.

7.2 Phased Array Configuration

The proposed phased array is simply implemented using one substrate of dielectric constant ε_r and thickness *h*. Rectangular patches of side length *a* are printed on the top conductor layer of the substrate while being fed through probes, as shown in Figure **7.1**. Meanwhile, the top conductor layer has square openings of side length *2R* around the patch. Many via holes spaced along those square openings are drilled in the substrate and are through platted constituting the SIW cavities backing each radiating element, as shown in Figure **7.1**.

To that end, the design of the SIW cavity-backed patch phased array typically involves the selection of the properties of the substrate (thickness and dielectric constant) and the dimensions of the patches and cavities. The substrate properties basically determine the scan performance and the bandwidth of the phased array. In the next sections, detailed design guidelines will be given.



(a)

(b)

Figure 7.1 Proposed SIW cavity-backed patch phased array (patches are fed by SMAs, not shown in figure, and probes are assumed to be in the middle of patches). (a) Top view. (b) Section view.

7.3 Scan Performance

We have numerically investigated the scan performance of the proposed phased arrays by carrying out a thorough parametric study using CST Microwave Studio [101]. We have assumed in the numerical study, that the phased array is infinite utilizing the periodic boundary conditions of CST to simulate just a unit cell of the array. We have then calculated the active reflection coefficient of the proposed phased arrays versus the scan angle for various substrate properties varying both the dielectric constant and the thickness of the substrate. Array spacing of $0.5\lambda_0$ was assumed in our study.

Starting by a low dielectric constant substrate of ε_r=2.2, Figure **7.2**-4 show the simulated active reflection coefficient versus scan angle of both the proposed SIW and the microstrip phased arrays for various substrate thicknesses namely; h=$0.026\lambda_0$, h=$0.052\ \lambda_0$ and h=$0.106\lambda_0$, respectively.

For the relatively thin substrate (h=$0.026\lambda_0$), it is clear that the scan performance of the proposed SIW phased array is little different to that of the microstrip phased array in both E- and H-planes since the cavity has not much effect yet. It is worth noting here that the scan range in both arrays is H-plane limited to 51º, as shown in Figure **7.2**. Upon increasing the substrate thickness to $0.052\lambda_0$, the cavity effect starts to appear and both the E- and H-planes scan ranges are increased to 70º, and 60º, respectively as shown in Figure **7.3**. Also, there is performance peak near end-fire, which an indication of leaky wave mode propagation. At this substrate thickness the array is still H-plane limited. Further increase of the substrate thickness to $0.106\lambda_0$, substantially extends the scan range in E- and H-planes to 75º, and 83º, respectively, as shown in Figure **7.4**(a). However, in this case the scan range of both phased arrays is E-plane limited which is consistent with the performance of metalized cavity-backed patch phased array demonstrated before in [47, 99].

It is worth noting also here, that we managed to obtain a relatively low reflection at broadside by tuning the position of the feeding probe without the need for adding a matching network, which considerably simplifies the structure. Figure **7.4** shows for instance both the scan performance of the phased array in case of ε_r=2.2 and h=$0.106\lambda_0$ with and without broadside matching. It is clear that both (with and without matching) have similar scan range for either the microstrip or the SIW case.

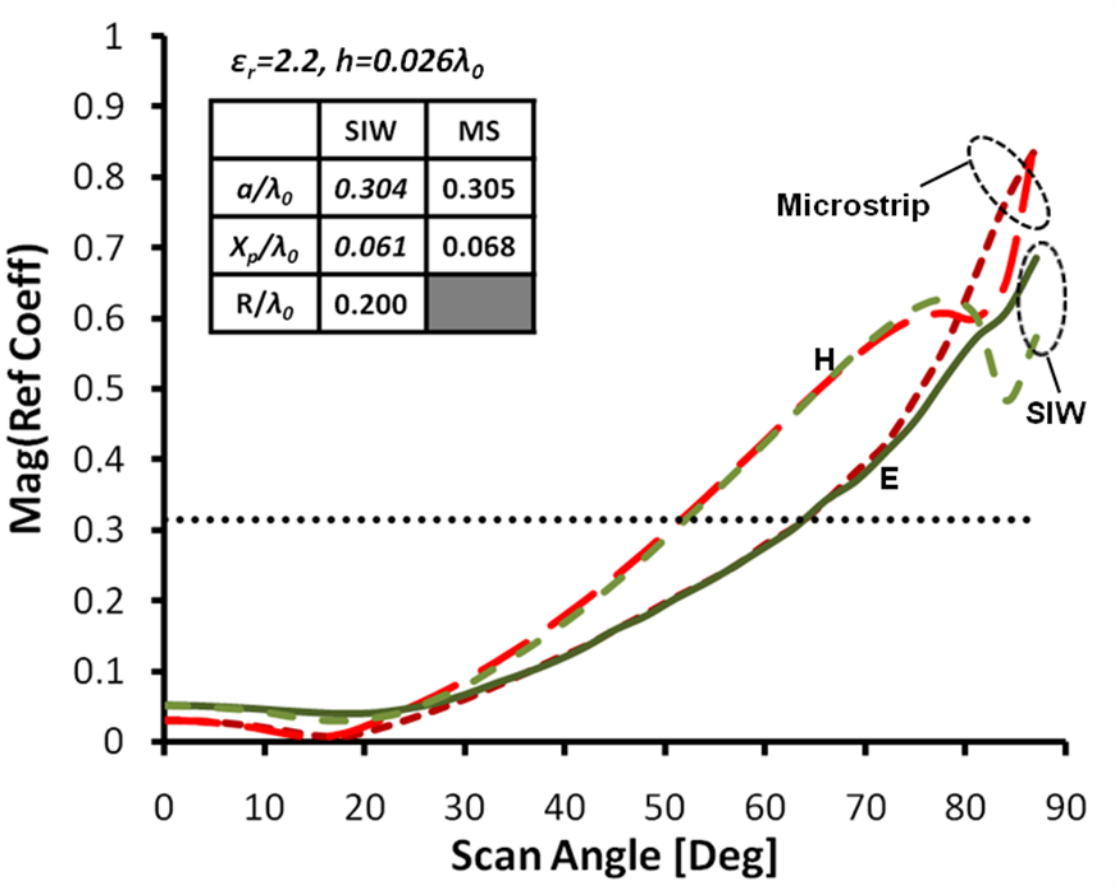


Figure 7.2 Simulated active reflection coefficient vs. scan angle of the SIW cavity-backed phased array compared to the microstrip array for both the E- and H- planes (assuming ε_r=2.2and h=0.026λ_0).

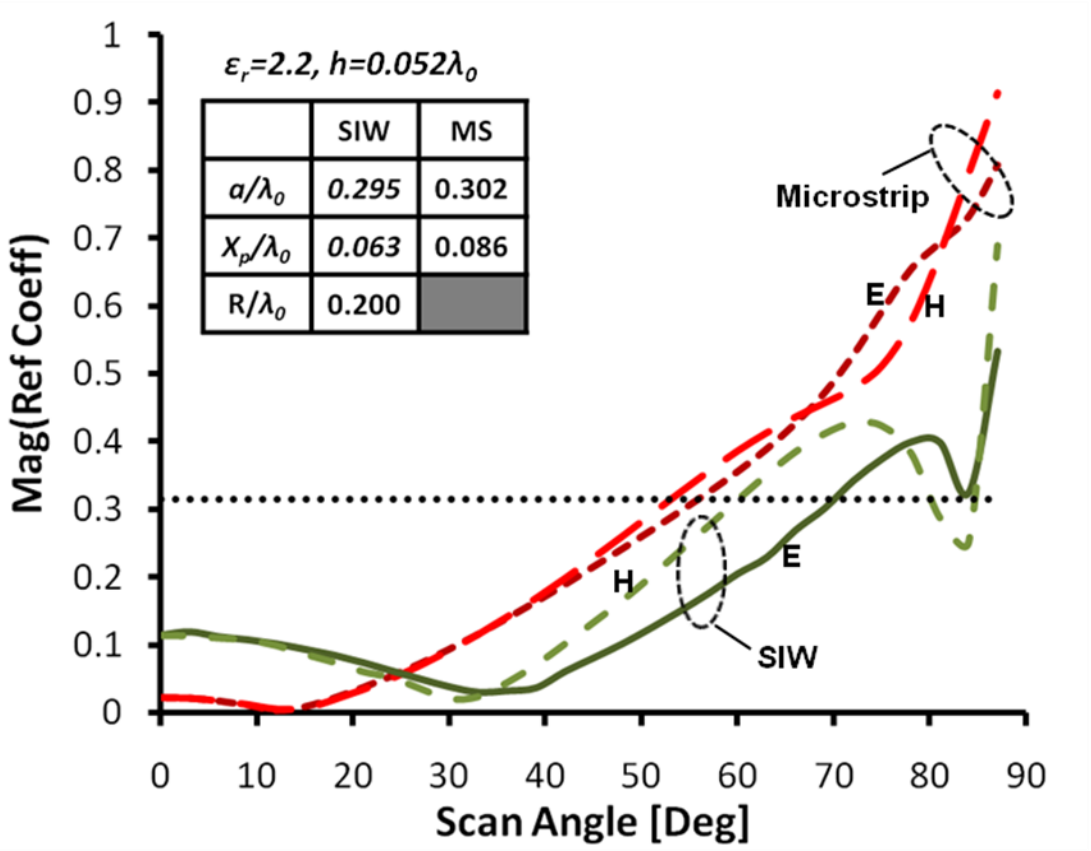
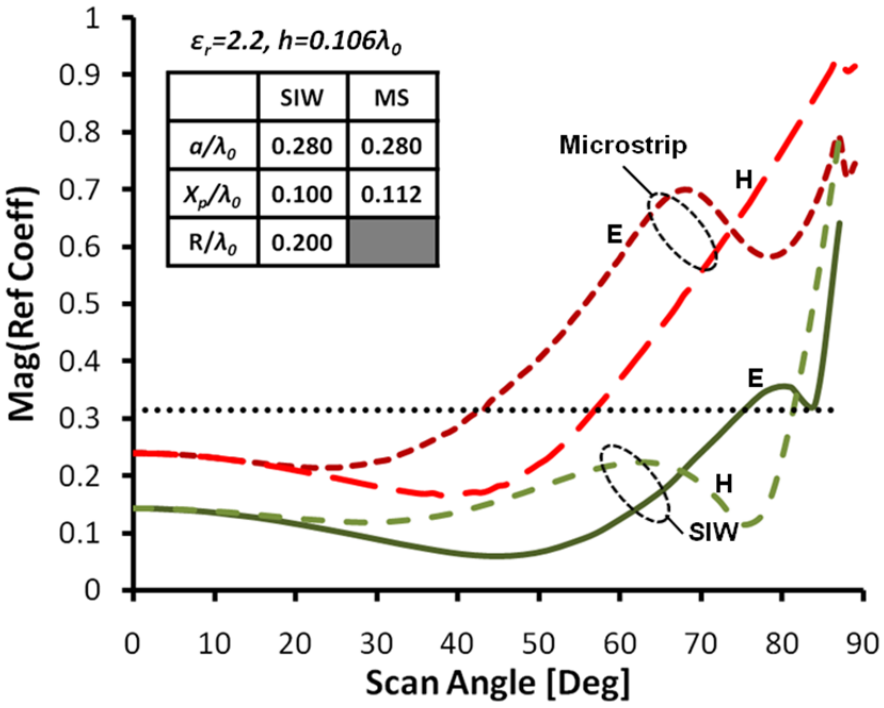


Figure 7.3 Simulated active reflection coefficient vs. scan angle of the SIW cavity-backed phased array compared to the microstrip array for both the E- and H- planes (assuming ε_r=2.2and h=0.052λ_0).

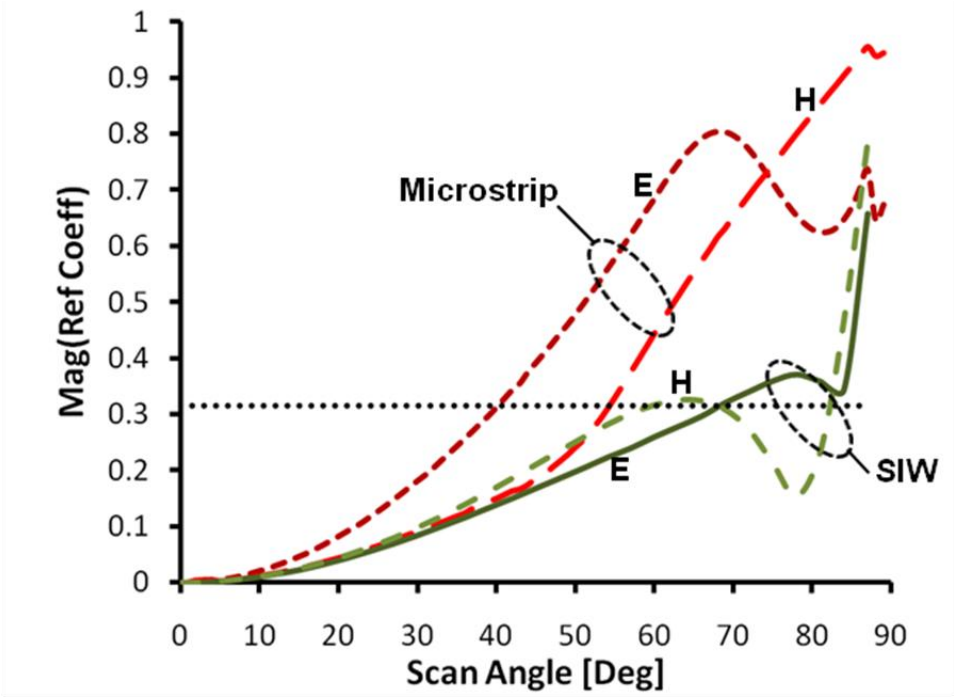
Meanwhile, the fractional bandwidth (-10 dB bandwidth of S_{11} normalized to the center frequency) of the SIW cavity-backed phased array increases from 4% to 8%, then to 12% upon increasing the substrate thicknesses from 0.026λ_0 to 0.052λ_0, and 0.106λ_0, respectively as shown in Figure **7.5**. This is expected as the bandwidth is generally proportional to the antenna volume and so to the substrate thickness.

We have also studied the scan performance in other cases where the dielectric constant of the substrate was set to relatively higher values of ε_r=4.5 and 6.0, while keeping a substrate thickness of h=0.106λ_0, as shown in Figure **7.6** and 7.7, respectively. It is clear that increasing the dielectric constant would seriously affect the scan performance of the microstrip phased arrays especially in the E-plane, while the use of SIW phased array would lead to relatively wider scan performance.

For instance, using the ε_r=4.5 substrate limits the scan range of the microstrip array to only 35º, and 57º compared to 60º and 75º when using the SIW structure for the E- and H-plane, respectively as shown in Figure **7.6**(a). Here, again the scan range of both the microstrip and SIW arrays are E-plane limited. Meanwhile, again with and without broadside matching are relatively similar in scan range.



(a)



(b)

Figure 7.4 Simulated active reflection coefficient vs. scan angle of the SIW cavity-backed phased array compared to the microstrip array for both the E- and H- planes (assuming ε_r=2.2and h=0.106λ_0). (a) Without matching at broadside. (b) Broadside matched.

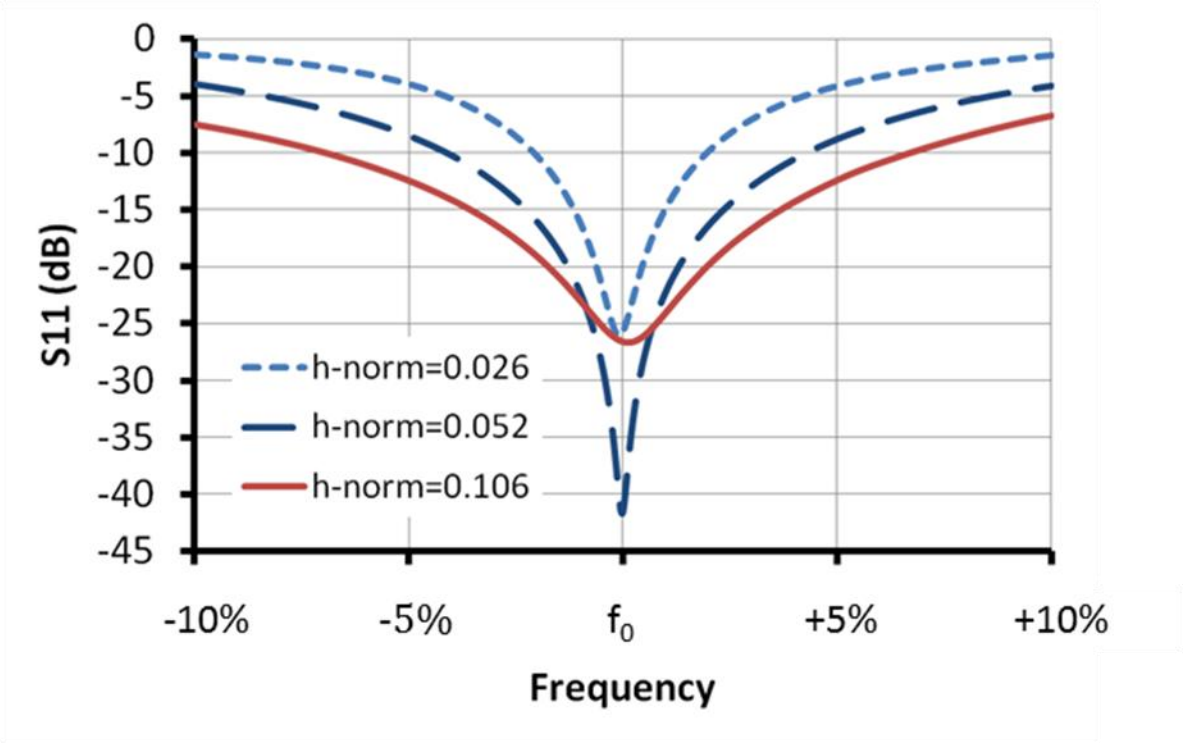
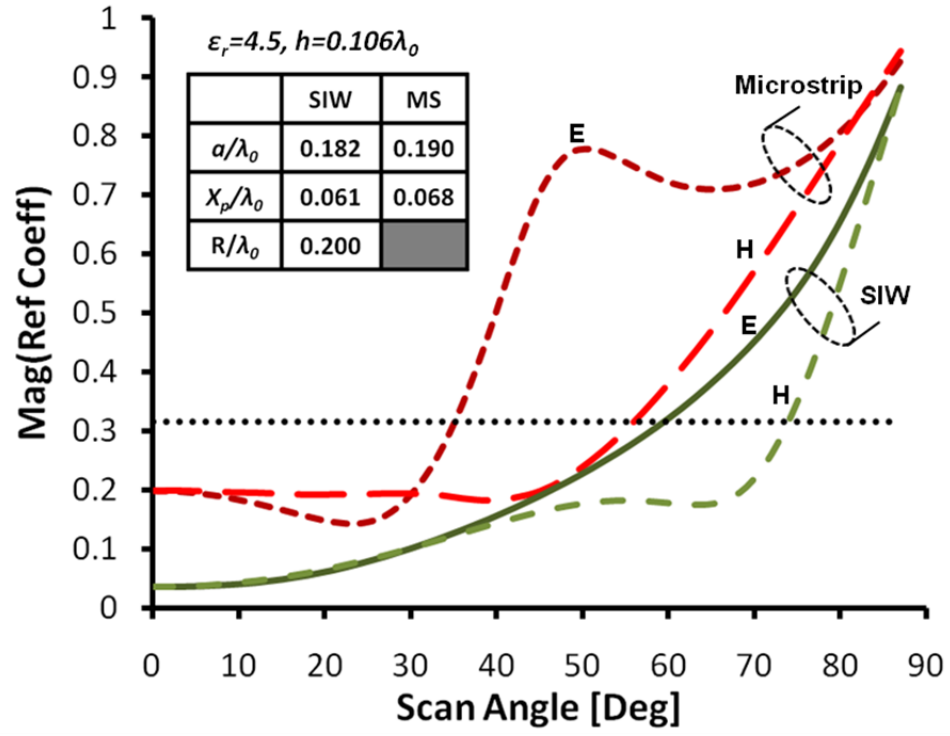
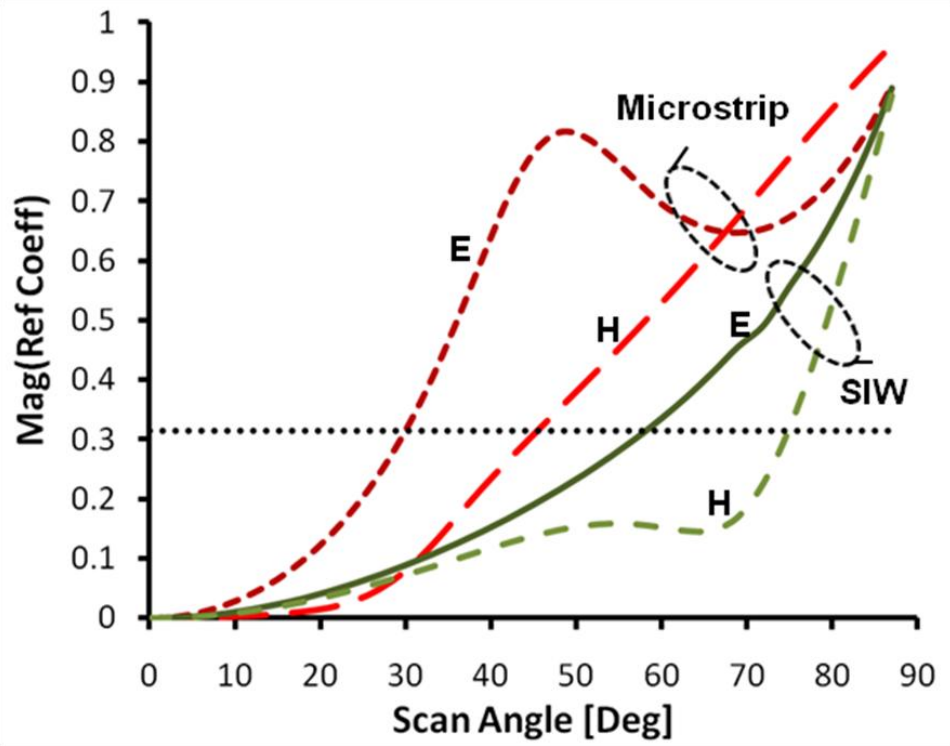


Figure 7.5 Simulated reflection response of the SIW cavity backed patch and microstrip phased arrays assuming ε_r=2.2 for different substrate thicknesses (h=0.026λ_0, h=0.052λ_0, and h=0.106λ_0).

Finally, using the ε_r=6.0 substrate would seriously limits the san range of the microstrip array to even narrower value of only 23º in the E-plane, while the scan range in the H-plane is about 60º, as shown in Figure **7.7**(a). That very limited scan range in the E-plane is not acceptable and would really impede using such an array in most phased array applications. On the other hand the scan range of the corresponding SIW array is 65º and 57º in the E- and H-plane, respectively which is much better when compared to the microstrip case. It is interesting to notice here that the SIW array is not actually E-plane scan limited but is H-plane limited in scan range. Meanwhile, matching at broadside slightly degrade the scan range in this case as shown in Figure **7.7**(b).

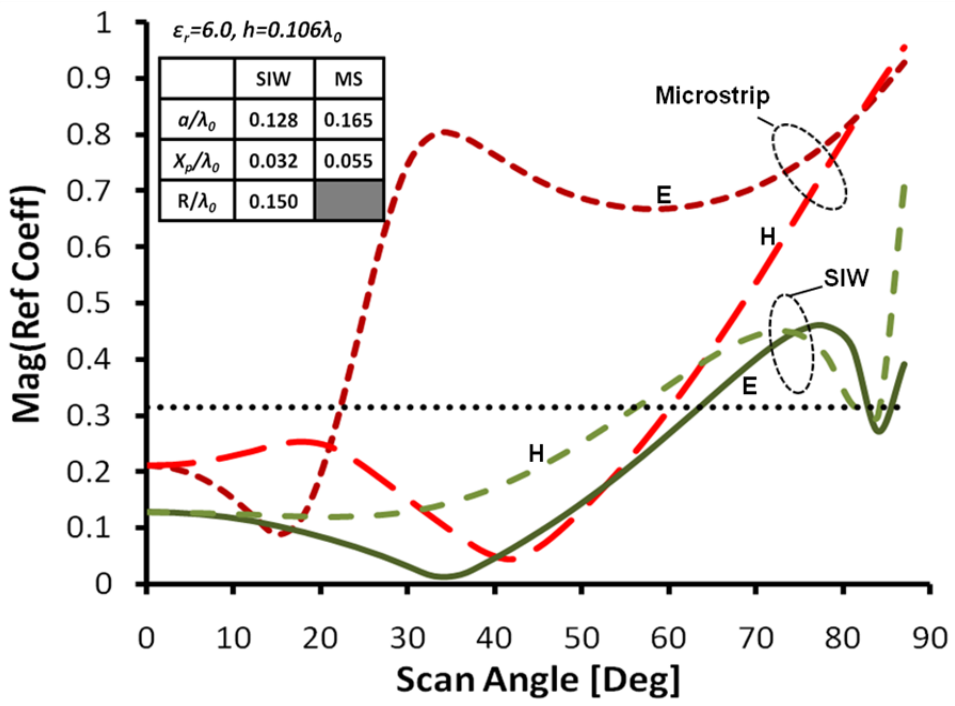


(a)

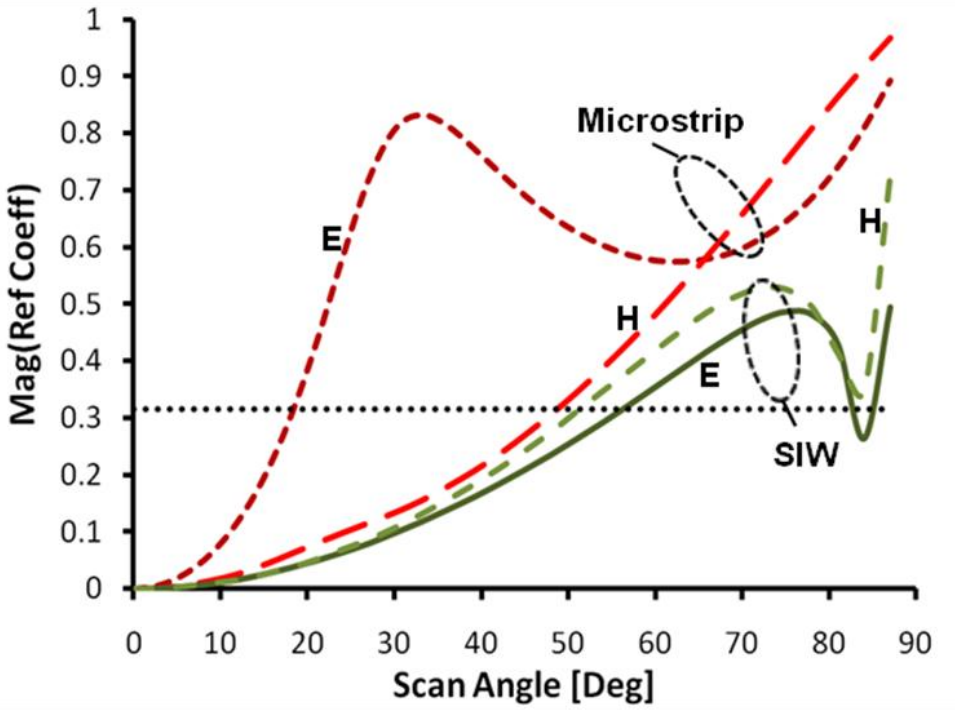


(b)

Figure 7.6 Simulated active reflection coefficient vs. scan angle of the SIW cavity-backed phased array compared to the microstrip array for both the E- and H- planes (assuming ε_r=4.5and h=0.106λ_0). (a) Without matching at broadside. (b) Broadside matched.



(a)



(b)

Figure 7.7 Simulated active reflection coefficient vs. scan angle of the SIW cavity-backed phased array compared to the microstrip array for both the E- and H- planes (assuming ε_r=6.0and h=0.106λ_0). (a) Without matching at broadside. (b) Broadside matched.

We have then carried out extensive numerical study to find out the scan range both in E- and H-planes of the proposed SIW cavity-backed patch phased array versus the normalized substrate thickness. Figure **7.8**-10 show our findings for various dielectric constant values. It is clear that generally the SIW arrays exhibit wider scan range rather than the microstrip arrays, which even gets better upon increasing the substrate thickness in contrary to the microstrip case, where the scan range in E-plane gets worse with increasing the thickness. It is worth mentioning also that the scan range starts from being H-plane limited at relatively small thicknesses and cross over to be E-plane limited for relatively thicker substrates. That happened for both cases of using ε_r=2.2 and ε_r=4.5, as shown in Figure **7.8**-9 but didn't happen in our range of substrate thicknesses for the case of using ε_r=6.0, where the SIW array is still H-plane limited in scan range even at h=0.106λ_0, as shown in Figure **7.10**, however it is expected to eventually cross-over at thicker value of the substrate thickness.

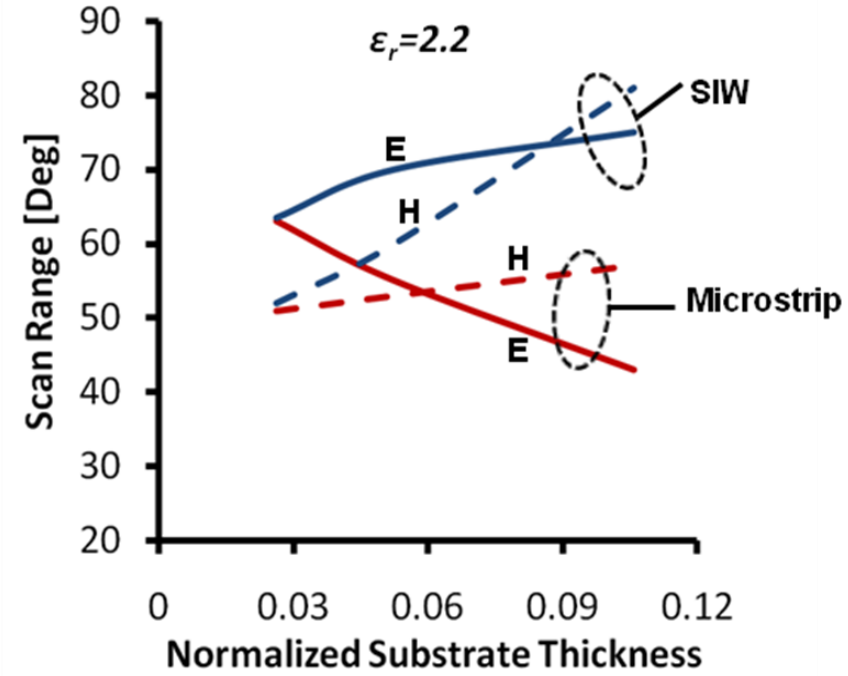


Figure 7.8 Simulated scan performance vs. normalized substrate thickness of the SIW cavity-backed patch and the microstrip phased arrays assuming ε_r=2.2.

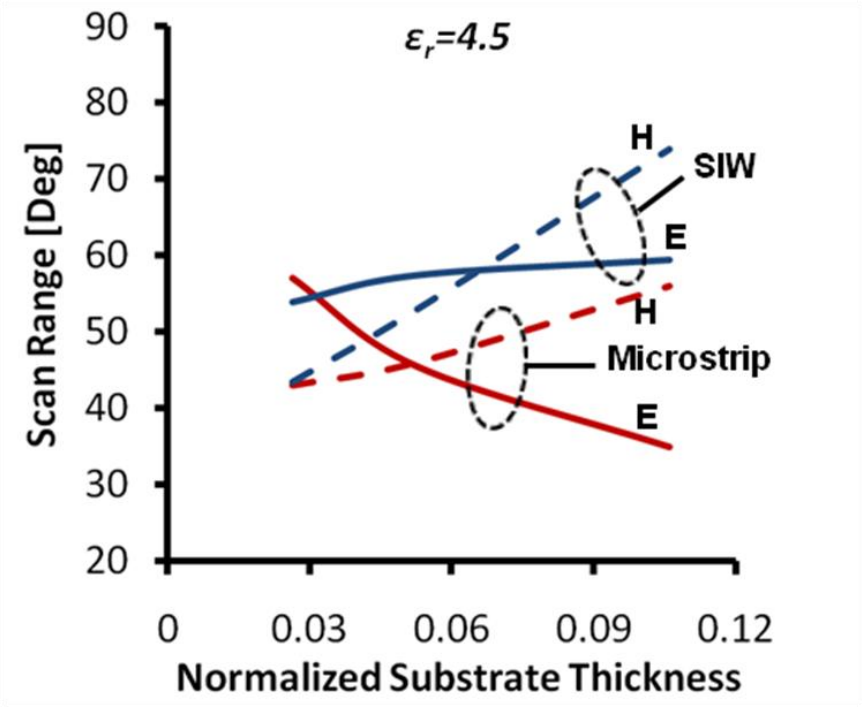


Figure 7.9 Simulated scan performance vs. normalized substrate thickness of the SIW cavity-backed patch and the microstrip phased arrays assuming ε_r=4.5.

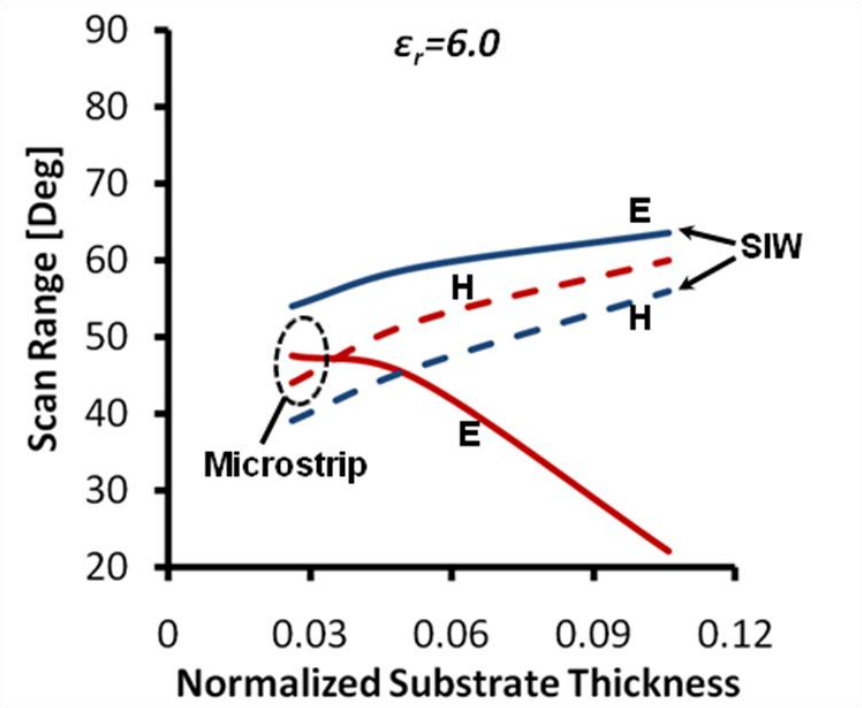


Figure 7.10 Simulated scan performance vs. normalized substrate thickness of the SIW cavity-backed patch and the microstrip phased arrays assuming ε_r=6.0.

7.4 Design Guidelines

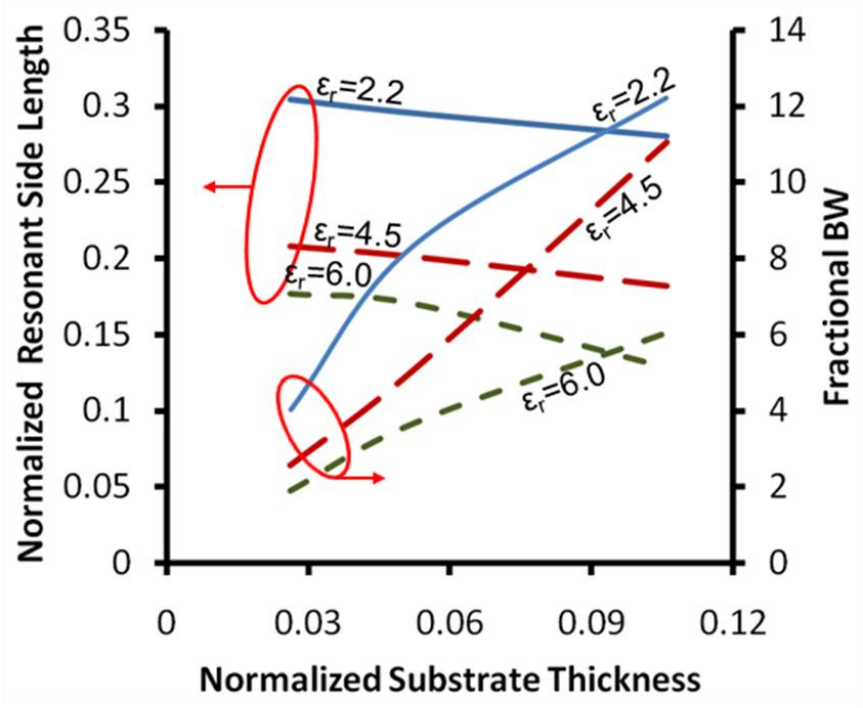
As mentioned before, the design of the SIW cavity-backed patch phased array involves the selection of substrate properties (dielectric constant and thickness) given the required overall scan range and fractional bandwidth, then determining the patch, cavity dimensions and probe position in order to achieve good matching performance.

We have then quantified the expected fractional bandwidth (as defined before -10 dB bandwidth of S_{11} normalized to the center frequency) of the proposed SIW array versus the normalized substrate thickness, as shown in Figure **7.11**(a). As expected and demonstrated before the fractional bandwidth is proportional to the substrate thickness while it is inversely proportional to the square root of the dielectric constant of the substrate.

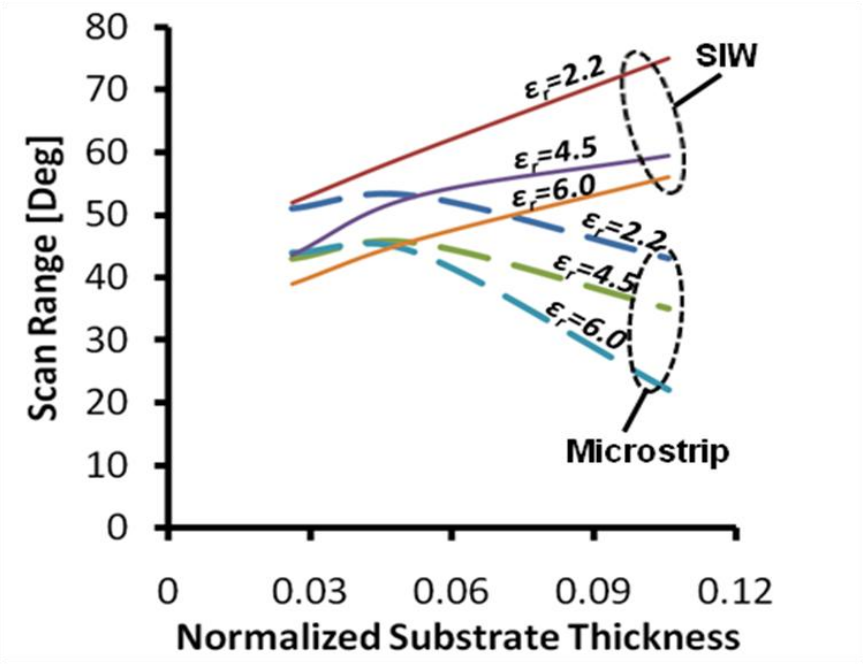
Meanwhile, the resonant side length of the patches is also shown in Figure **7.11**(a). It is clear that increasing the dielectric constant of the substrate has again a miniaturization effect on the patches size, as expected. Increasing the substrate thickness has also some miniaturization effect. That is consistent with our previous experience with the fixed beam arrays demonstrated before in Chapter 3.

On the other hand, Figure **7.11**(b) shows the overall scan performance of the proposed SIW phased arrays defined as the smaller of the E- and H-plane scan ranges. It is very interesting to notice how the proposed arrays are far superior to the microstrip ones in overall scan range and how the scan range of the SIW arrays gets better with increasing the substrate thickness.

The design charts, shown in Figure **7.11**, would be very helpful in attaining phased arrays of the proposed topology to meet certain scan range and bandwidth requirements. We have used it to design a phased array of scan range larger than 60º and fractional bandwidth better than 12%. We have used low dielectric constant thick substrate of ε_r=2.2 and $0.106\lambda_0$. The final dimension of the structure is as follows: array spacing $d=0.5\lambda_0$, patch size $a=0.28\lambda_0$, cavity side length $2R=0.4\lambda_0$, and probe location $x_p=a/2.8$ (the same case studied before and its simulated scan range is shown in Figure **7.4**).



(a)



(b)

Figure 7.11 Design chart for the proposed SIW cavity-backed patch phased array. (a) The fractional bandwidth and the normalized resonant side length vs. normalized substrate thickness for various substrate dielectric constants. (b) Overall scan range (smaller of the E- and H-plane scan ranges) vs. normalized substrate thickness of the proposed array compared to the microstrip array.

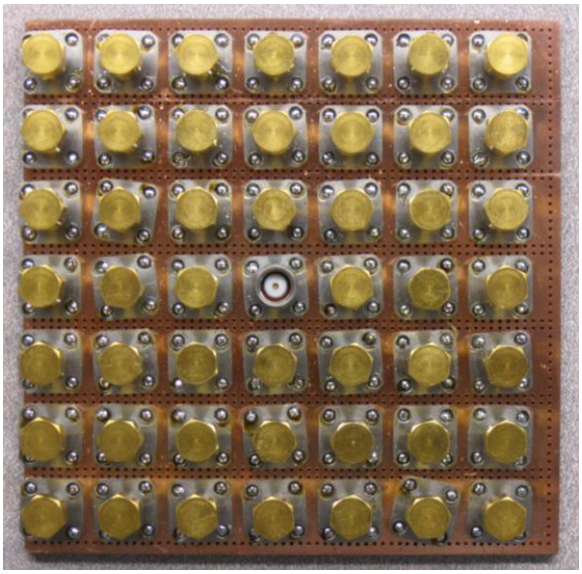
7.5 Experimental Results

A 7x7 array of the designed SIW cavity-backed patch phased array has been fabricated, as shown in Figure **7.12**. Rogers RT/duroid 5880 substrate with a relative dielectric constant of 2.2 and a thickness of 3.175 mm was utilized to build both the SIW and microstrip arrays. Figure **7.12**(a) shows the top view of the structure depicting the patches and the SIW cavities, emulated by the platted via holes. Standard SMAs of solder cup contacts were utilized in launching the signal to the different array probes and were then matched by standard SMA 50Ω terminations except the center port and thus attaining the matched array environment, as shown in Figure **7.12**(b).

Figure **7.13** shows the normalized measured E-plane active gain patterns of the proposed SIW cavity-backed array (solid), and of the corresponding microstrip array (dashed) compared to that of the ideal cos(θ) patterns (dotted). Clearly the proposed SIW phased array has a wider pattern when compared to the microstrip array pattern and it is clear from any scan blindness, while the microstrip array seems to have a kind of week scan blindness at about 35º. The SIW cavity-backed patch phased array pattern is pretty close to the ideal cos(θ) pattern. That evidently proves the proposed array potential in extending the limited scan range of conventional microstrip arrays.

In fact, the measured active gain of the microstrip array is relatively worse than expected from simulation, shown before in Figure **7.4**. An independent HFSS simulation for the 7x7 finite microstrip array has been carried out to investigate further the performance of the microstrip array. Figure **7.14** shows the HFSS model used in our investigation. The simulated versus measured E-plane active normalized gain of the finite 7x7 microstrip phased array is shown in Figure **7.15**. Similar scan trends to the measured performance could be predicted using the finite array model (except of that shoulder approximately at 50º). We conclude that the relatively worse than expected performance of the microstrip array is attributed to the edge effects of the finite array.

(a)



(b)

Figure 7.12 Picture of the fabricated SIW cavity-backed patch 7x7 phased array. (a) Top view showing the patches and the SIW cavities emulated by the platted via holes. (b) Bottom view showing the array in a matched array environment.

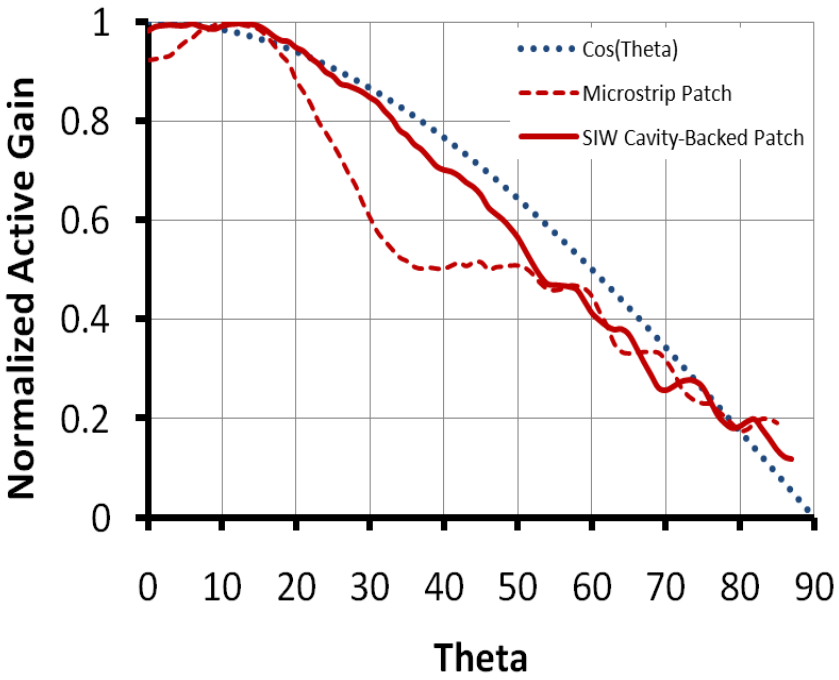


Figure 7.13 Normalized measured E-plane active gain pattern of the SIW cavity-backed (solid), and the microstrip patch (dashed) 7x7 phased arrays compared to the ideal cos(θ) pattern (dotted).

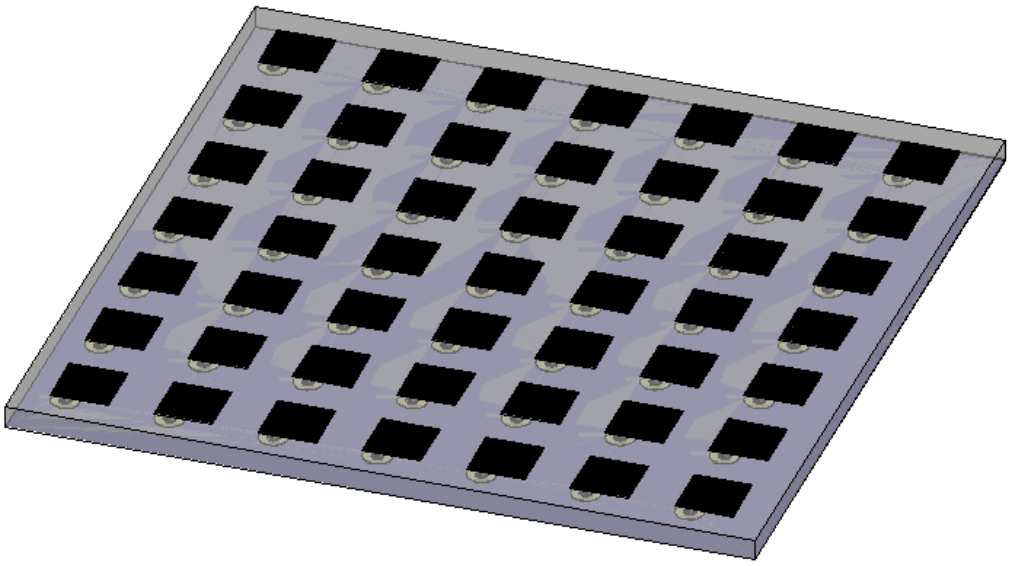


Figure 7.14 HFSS model of the 7x7 finite microstrip array.

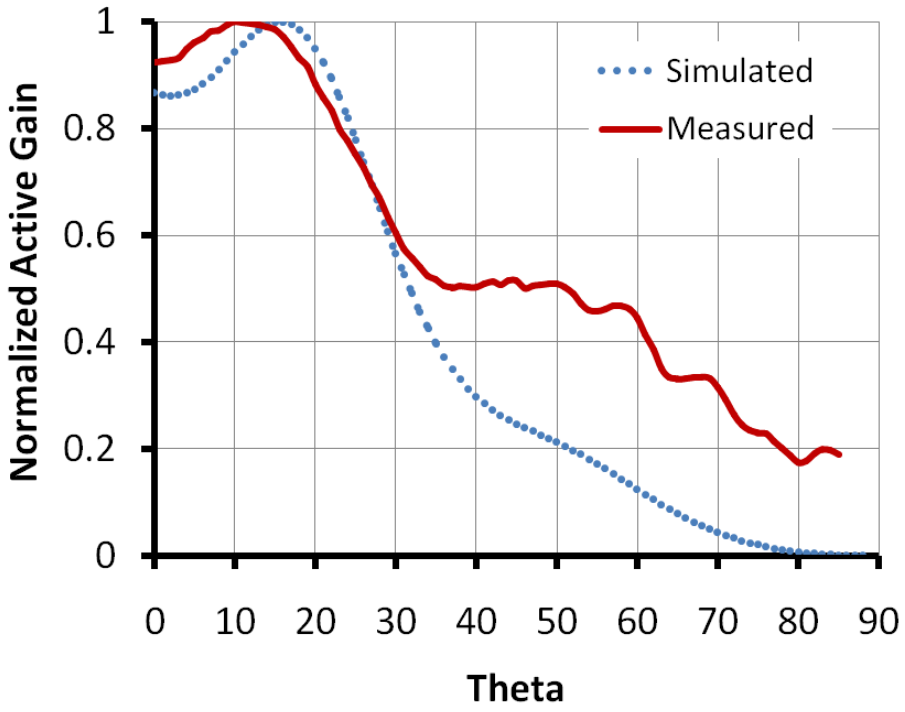


Figure 7.15 Simulated versus measured E-plane normalized active gain of the 7x7 finite microstrip array.

7.6 Conclusion

SIW technology proved useful in attaining low-cost, wide-band, and wide-scan angle cavity-backed patch phased arrays. The scan performance of the proposed arrays is substantially wider than that of the conventional microstrip patch phased arrays. Moreover, increasing the substrate thickness secures both better scan performance and wider bandwidth for the cavity-backed patch phased array, in contrast to that of the microstrip phased array which has significantly limited scan range upon increasing the substrate thickness. A 7x7 phased array of the proposed structure has been fabricated and tested in a matched array environment. Results indicated the suitability of the proposed approach in attaining a phased array with relatively wide bandwidth of 12%, and with wide scan performance of better than 60º free from any scan blindness.

Chapter 8 Conclusion and Future Work

8.1 Research Efforts Summary

We have carried out extensive study on cavity-backed patch antennas. Our efforts were aimed at bandwidth enhancement, low cost implementation, and achieving maximum gain performance. For bandwidth enhancement, we have avoided using thick microstrip feed networks to minimize surface wave propagation, and only backed the patches by adequate deep cavities to increase the patch antenna volume, and so increases its operating bandwidth. Presence of periodic cavities should also enhance surface wave suppression. For low cost implementation, we have used substrate-integrated waveguides which can be utilized for multi-layer RF structures. SIW technology offers fast prototyping, low cost implementation, and accurate metal pattern definition. For maximum gain, we have investigated the use of circular patches rather than rectangular patches and emphasized the use of low loss feed networks. In our investigations, we pursued both theoretical and experimental routes to understand the performance of the cavity-backed patch antenna structures and develop design guideline rules.

Full EM analysis was carried out for both 2D microstrip and cavity-backed patch antennas. The 2D microstrip antenna analysis was based on Liu's analysis, which was extended for cavity-backed patches. Results indicated that wider bandwidth and wider scanning range can be achieved when adding the backing cavities. The 2D analysis was compared to results obtained using commercially available CAD tools "CST and HFSS", subsequently 3D analysis was carried out using HFSS and CST and were experimentally validated as well.

Experimentally, we have utilized single layer structures of cavity-backed patch antennas that were fed using individual coaxial SMA connectors. This simple structure was used to demonstrate scanning range and evaluation of cavity scanning enhancement. Meanwhile, for real antenna implementation a microstrip binary feed network was utilized, however it required adding another layer. Good efficiency performance of over 70% was demonstrated for antennas up to 4x4, however significant efficiency drop was seen for 8x8 arrays due to the significant loss of the microstrip feed network. We tried to replace the microstrip feed network by a waveguide feed network to reduce the insertion loss and attain dual polarization. But, it required using a third layer to implement the waveguide cooperate feed network. Practically, very slight improvement in performance was demonstrated due to the significant insertion loss of various transitions and the associated losses of the relatively long feed-thru along the three layers. Additionally, stacking three layers turns out to be problematic and using screws to hold the three layers is not adequate and caused pronounced unaccounted for losses, due to the presence of airgaps especially for the large arrays.

Subsequently, to build large arrays of cavity-backed patch, it is essential to develop relatively lower loss transitions, and new bonding methods of such three layer structures. Definitely, using metallic guides could be used instead of SIW but it is expensive.

8.2 Contributions

The contributions of the dissertation lies in the following:-

8.2.1 **SIW Cavity-Backed Arrays**

- Proposed the substrate-integrated cavity-backed topology as an alternative low-cost approach for bandwidth enhancement.
- Evaluated the proposed topology against the conventional bandwidth enhancement techniques.
- Produced design charts that could be utilized in attaining similar arrays with different specs.

8.2.2 **Dual-Polarized Array**

- Extended the SIW-cavity backed patch array topology to include dual linear polarization.

8.2.3 **Phased Array**

- Analyzed the cavity-backed patch arrays using a simplified 2-D analysis.
- Utilized the SIW cavity-backed topology to attain wide-band wide-scan angle phased array.
- Experimentally demonstrated the performance of the proposed phased array.

8.3 Publications

8.3.1 **Journal Papers**

1) **M. H. Awida**, Shady F. Suleiman, A. E. Fathy, "**Substrate-Integrated Cavity-Backed Patch Arrays: A Low-Cost Approach for Bandwidth Enhancement**," *IEEE Antenna and Propagation Trans.*, vol. 59, pp. 1155-1163, 2011
2) **M. H. Awida**, A. E. Fathy, "**Substrate-Integrated Waveguide Ku-Band Cavity-Backed 2x2 Microstrip Patch Array Antenna**," *IEEE Antennas and Wireless Propagation Letters*, vol. 8, pp. 1054-1056, 2009.

8.3.2 **Conference Papers**

1) **M. H. Awida,** E. Elkhouly**,** A. E. Fathy, **"Low-Cost High-Efficiency Substrate-Integrated Cavity-Backed Single Element Antenna,"** *in APS Conference, Toronto, Jul. 2010.*
2) **M. H. Awida,** E. Elkhouly**,** A. E. Fathy, **"A 2x4 Substrate-Integrated Waveguide Probe-Fed Cavity-Backed Patch Array,"** *in APS Conference, Toronto, Jul. 2010.*
3) **M. H. Awida,** Shady F. Suleiman**,** A. E. Fathy, **"Development of SIW Cavity-Backed Dual-Polarized Ku-Band Microstrip Patch Arrays,"** *in URSI Conference, Boulder, Colorado, Jan. 2010.*
4) **M. H. Awida,** Shady F. Suleiman**,** A. E. Fathy, **"Development of a Substrate-Integrated Ku-Band Cavity-Backed Microstrip Patch Sub-Array of Dual Linear/Circular Polarization for DBS Applications,"** *in IEEE Radio Wireless Symposium 2010.*
5) S. Yang**, M. H. Awida,** Shady F. Suleiman**,** A. E. Fathy, **"Low-Cost Low-Profile Dual Circularly Polarized Ku-Band Antennas for Mobile Satellite Platforms,"** in *Antenna Applications Symposium 2009.*
6) **M. H. Awida,** A.H Kamel, A. E. Fathy, **"On the Convergence of MoM for Infinite Phased Arrays,"** *in URSI Conference, Boulder, Colorado, Jan. 2008.*
7) A. E. Fathy, **M. H. Awida,** M. J. Kuhn, J. L. Wilson, **"Microwave Holographic Antennas,"** *in URSI Conference, Manitoba, July 2007.*

8.4 Conclusion

In this dissertation, a low-cost implementation of cavity-backed antennas has been proposed and experimentally verified using substrate-integrated waveguide (SIW) technology. Beginning with single element antennas, four different single elements corresponding to the different combinations of patch and cavity shapes have been fabricated and experimentally tested. The proposed cavity-backed patch antenna elements are comprised of only a single substrate where a patch is printed on the top substrate surface; while the cavity is implemented using plated via holes to emulate the conventional metalized cavities to back and surround the patches. The shape of the patch and cavity has noticeable effect on the bandwidth and x-pol performance of such elements. Developed design charts of the investigated four permutations of circular and rectangular structures have indicated that the substrate thickness (cavity height) could be selected to attain a given bandwidth for the patch up to 15% without degrading the patch efficiency as the surface waves are suppressed by the SIW cavity. The different fabricated prototypes have demonstrated

fractional bandwidth larger than 9% and realized gain higher than 8dBi, corresponding to more than 80% in aperture efficiency. Circular patches tend to give better bandwidth while the rectangular patches tend to give better cross-pol. On the other hand, the circular cavities tend to secure lower mutual coupling. Circular patch backed by circular cavity exhibits the highest gain of 8.6 dBi corresponding to 92% aperture efficiency.

Moving to large arrays, the proposed SIW cavity-backed topology has been utilized in attaining microstirp-fed arrays that consist of a stack of two substrates: the top substrate for the patches and microstrip feed network and the bottom one for the SIW cavities. The top microstrip substrate should be kept thin in order to minimize the surface waves and the associated feed network losses. Meanwhile, the bottom cavity substrate should be relatively thick for bandwidth enhancement. A design chart for the basic 2x2 sub-array has been presented and used with a modular design approach to realize larger arrays. The proposed SIW cavity-backed arrays outperform both the thick microstrip and suspended arrays in terms of gain and aperture efficiency. The SIW structure has a comparable performance to the cavity-backed suspended arrays and the conventional metalized cavity-backed arrays, but with a much lower fabrication cost. Various SIW cavity-backed microstrip-fed array prototypes have been fabricated and experimentally tested. The fabricated structures, as predicted, have very good radiation characteristics, enhanced bandwidth, and high aperture efficiency up to 4x4 size arrays. But, once we get to arrays with 8x8 elements, significant gain drop was noticed. The overall gain drop for the 8x8 array is related to excessive feed loss and assembly problems.

For further performance enhancement, substrate-integrated waveguide feed networks have been utilized to substantially lower the dominant loss contributor; i.e. the feed loss and improve the efficiency of large arrays. The substrate-integrated waveguide feed offers the potential to lower the relatively higher losses associated with the long microstrip feed lines, yet at much lower cost when compared to the conventional waveguide feed topologies. Teaming up the SIW feed with the SIW cavities secures a potential antenna solution with relatively good bandwidth controlled by the cavity height and also good efficiency sustained by the SIW feed. However, the assemblage of SIW-fed array becomes more challenging as the array size gets larger.

The proposed SIW-fed array structure is also a good candidature for DBS applications with our proposed solution to attain dual polarization of operation. A Ku-band 4x16 cavity-backed microstrip patch array of dual linear/circular polarization has been developed based on substrate-integrated waveguide (SIW). The measured antenna array performance covers the DBS frequency range from 12.2 GHz to 12.7 GHz, exhibiting about 24.2 dBi, 24.3dBi for the horizontal and vertical polarization, respectively at 12.45 GHz. Poor match at the low frequency end, and some assembly problem as we only

used metal screws for holding the three layers, caused some gain pattern ripples of over 1 dB, especially at the lower frequency end. Even though the gain improvement compared to the microstrip case is not significant, but this SIW-fed structure can render dual polarization. The developed array constitutes a good basic panel for larger array designs along with an SIW feed network, however, it would require significant improvements in various transition performance and a more robust method for stacking the three layers.

On the other hand the SIW cavity-backed topology has been also proposed as a solution to resolve the limited scan range problem of the conventional microstrip phased arrays. To qualitatively evaluate the potential of the proposed cavity-backed topology, a simplified 2-D analysis to both the microstrip and cavity-backed patch phased arrays has been carried out to initially investigate the scan range in each case. Using the 2-D analysis, the E-plane scan performance of the cavity-backed patch array has been calculated for two distinctive cases; in the first, the structure is comprised of two substrates where the patch is printed on a separate substrate above another substrate where the cavity is implemented. The other case is comprised of just one substrate where the patch is printed on the top conductor of the cavity substrate. The numerically calculated scan performances qualitatively indicates the potential of using the cavities to impede the surface waves, thus enhancing the limited scan range exhibited by the conventional microstrip phased arrays.

Further studies of the scan performance in both E- and H-planes has been demonstrated using however commercial EM simulation tool (CST microwave studio), which proved SIW technology useful in attaining low-cost, wide-band, and wide-scan cavity-backed patch phased arrays. The scan performance of the proposed arrays is substantially wider than that of the conventional microstrip patch phased arrays. Moreover, increasing the substrate thickness secures both better scan performance and wider bandwidth for the cavity-backed patch phased array, in contrast to that of the microstrip phased array which has significantly limited scan range upon increasing the substrate thickness. A 7x7 phased array of the proposed structure has been fabricated and tested in a matched array environment. Results indicated the suitability of the proposed approach in attaining a phased array with relatively wide bandwidth of 12% and with wide scan performance of better than 60^{o} free from any scan blindness.

8.5 Future work

The future work of our research could be in the development of lower loss transition, and more robust assembly techniques to continue using SIW structure. On the other hand, investigating other fabrication techniques to build solid guides (like metal coated plastic structures) could be also explored to address the assembly problem.

Achieving the 32 dBi DBS antenna is quite challenging where many boards of high performance arrays should be cascaded and fed through a waveguide feed network. That is probably the natural extension of the work demonstrated in this dissertation.

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Appendices

Appendix A: Transmission Line Analysis of the 2-D Phased Arrays

In this appendix, the details of the transmission line analysis briefly described in Chapter 6 are given here.

A.1 Probe-Fed Microstrip Patch Phased Array

For the probe-fed patch phased array, the equivalent transmission line of the feed problem is shown again in Figure A.1, where

$$V_1(x) = v_1^+ e^{-jkx} + v_1^- e^{+jkx}$$
$$I_1(x) = \frac{v_1^+}{Z_1} e^{-jkx} - \frac{v_1^-}{Z_1} e^{+jkx}$$
$$V_2(x) = v_2^+ e^{-jk(x-x')} + v_2^- e^{+jk(x-x')}$$
$$I_2(x) = \frac{v_2^+}{Z_1} e^{-jk(x-x')} - \frac{v_2^-}{Z_1} e^{+jk(x-x')}$$

Then we have the following boundary conditions

1. $V_1(x') = V_2(x')$

   Which gives

$$v_1^+ e^{-jkx'} + v_1^- e^{+jkx'} = v_2^+ + v_2^-$$

2. $I_1(x') = I_2(x') - I_0$

   Which gives

$$v_1^+ e^{-jkx'} - v_1^- e^{+jkx'} = v_2^+ - v_2^- - I_0 Z_1$$

3. $V_1(0) = V_2(d) \cdot e^{j\delta}$

   Which gives

$$v_1^+ + v_1^- = \left(v_2^+ e^{-jk(d-x')} + v_2^- e^{+jk(d-x')}\right) e^{j\delta}$$

4. $I_1(0) = I_2(d) \cdot e^{j\delta}$

   Which gives

$$v_1^+ - v_1^- = \left(v_2^+ e^{-jk(d-x')} - v_2^- e^{jk(d-x')}\right) e^{j\delta}$$

The system of equations could be put in a matrix form as

$$Ax = b$$

$$A = \begin{pmatrix} e^{-jkx'} & e^{jkx'} & -1 & -1 \\ e^{-jkx'} & -e^{jkx'} & -1 & 1 \\ 1 & 1 & -e^{-j[k(d-x')-\delta]} & -e^{j[k(d-x')+\delta]} \\ 1 & -1 & -e^{-j[k(d-x')-\delta]} & e^{j[k(d-x')+\delta]} \end{pmatrix}$$

And

$$x = \begin{pmatrix} v_1^+ \\ v_1^- \\ v_2^+ \\ v_2^- \end{pmatrix}, \qquad b = \begin{pmatrix} 0 \\ -I_0 Z_1 \\ 0 \\ 0 \end{pmatrix}$$

Which could be solved to find v_1^+, v_1^-, v_2^+, and v_2^- and so the currents I_1 and I_2

Resulting in

$$I(x) = \begin{cases} \frac{I_0}{2}\left[\frac{e^{-j\delta-jk(x-x')}}{e^{-j\delta}-e^{-jkd}} - \frac{e^{-jk(d-x+x')}}{e^{j\delta}-e^{-jkd}}\right], x' < x < d \\ \frac{I_0}{2}\left[\frac{e^{-jk(d+x-x')}}{e^{-j\delta}-e^{-jkd}} - \frac{e^{j\delta+jk(x-x')}}{e^{j\delta}-e^{-jkd}}\right], 0 < x < x' \end{cases}$$

Similar to the expression in [5].

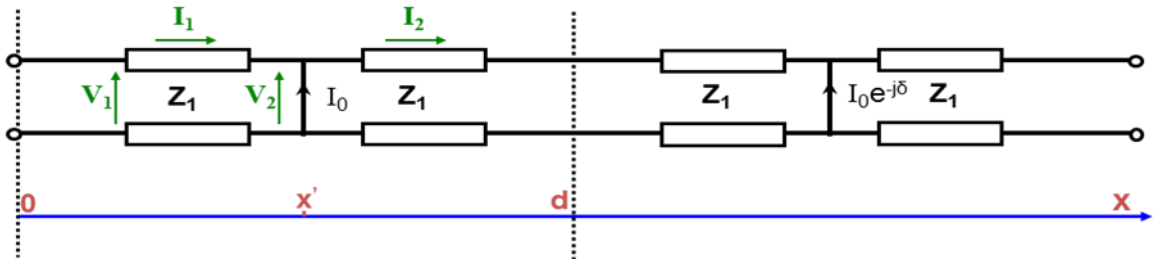

Figure A.1 Transmission line model of the feed problem of the probe-fed patch phased array.

A.2 Probe-Fed Cavity-Backed Patch Phased Array

Similarly, the cavity-backed phased array could be analyzed. The equivalent transmission line in this case consists of four sections as shown in Figure A.**2**

Again the voltages and currents could be written in terms of the incident and reflection voltage coefficients

$$V_1(x) = v_1^{+} e^{-jkx} + v_1^{-} e^{+jkx}$$

$$I_1(x) = \frac{v_1^{+}}{Z_1} e^{-jkx} - \frac{v_1^{-}}{Z_1} e^{+jkx}$$

$$V_2(x) = v_2^{+} e^{-jk(x-x_0)} + v_2^{-} e^{+jk(x-x_0)}$$

$$I_2(x) = \frac{v_2^{+}}{Z_2} e^{-jk(x-x_0)} - \frac{v_2^{-}}{Z_2} e^{+jk(x-x_0)}$$

$$V_3(x) = v_3^{+} e^{-jk(x-x')} + v_3^{-} e^{+jk(x-x')}$$

$$I_3(x) = \frac{v_3^{+}}{Z_2} e^{-jk(x-x')} - \frac{v_3^{-}}{Z_2} e^{+jk(x-x')}$$

$$V_4(x) = v_4^{+} e^{-jk(x-x_c)} + v_4^{-} e^{+jk(x-x_c)}$$

$$I_4(x) = \frac{v_4^{+}}{Z_1} e^{-jk(x-x_c)} - \frac{v_4^{-}}{Z_1} e^{+jk(x-x_c)}$$

Then applying the following boundary conditions:-

1. $V_1(x_0) = V_2(x_0)$
2. $I_1(x_0) = I_2(x_0)$
3. $V_2(x') = V_3(x')$
4. $I_2(x') = I_3(x') - I_0$
5. $V_3(x_c) = V_4(x_c)$
6. $I_3(x_c) = I_4(x_c)$
7. $V_1(0) = V_4(d) \cdot e^{j\delta}$
8. $I_1(0) = I_4(d) \cdot e^{j\delta}$

The resultant system of equations could be put in a matrix form as

$$Ax = b$$

Where

$$A=\begin{pmatrix} e^{-jkx_o} & e^{jkx_o} & -1 & -1 & 0 & 0 & 0 & 0 \\ e^{-jkx_o} & -e^{jkx_o} & -Z_1/Z_2 & Z_1/Z_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & e^{-jk(x'-x_o)} & e^{jk(x'-x_o)} & -1 & -1 & 0 & 0 \\ 0 & 0 & e^{-jk(x'-x_o)} & -e^{jk(x'-x_o)} & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & e^{-jk(x_c-x')} & e^{jk(x_c-x')} & -1 & -1 \\ 0 & 0 & 0 & 0 & e^{-jk(x_c-x')} & -e^{jk(x_c-x')} & -Z_2/Z_1 & Z_2/Z_1 \\ 1 & 1 & 0 & 0 & 0 & 0 & -e^{-j[k(d-x_c)-\delta]} & -e^{j[k(d-x_c)+\delta]} \\ 1 & -1 & 0 & 0 & 0 & 0 & -e^{-j[k(d-x_c)-\delta]} & e^{j[k(d-x_c)+\delta]} \end{pmatrix}$$

$$x=\begin{pmatrix} v_1^+ \\ v_1^- \\ v_2^+ \\ v_2^- \\ v_3^+ \\ v_3^- \\ v_4^+ \\ v_4^- \end{pmatrix} \qquad b=\begin{pmatrix} 0 \\ 0 \\ 0 \\ -I_0Z_2 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

Solving the system of equations gives the current as

$$I(x)=\begin{cases} \dfrac{v_1^+}{Z_1}e^{-jkx}-\dfrac{v_1^-}{Z_1}e^{jkx} & 0\le x<x_o \\ \dfrac{v_2^+}{Z_2}e^{-jk(x-x_o)}-\dfrac{v_2^-}{Z_2}e^{jk(x-x_o)} & x_o\le x<x' \\ \dfrac{v_3^+}{Z_2}e^{-jk(x-x')}-\dfrac{v_3^-}{Z_2}e^{jk(x-x')} & x'\le x<x_c \\ \dfrac{v_4^+}{Z_1}e^{-jk(x-x_c)}-\dfrac{v_4^-}{Z_1}e^{jk(x-x_c)} & x_c\le x<d \end{cases}$$

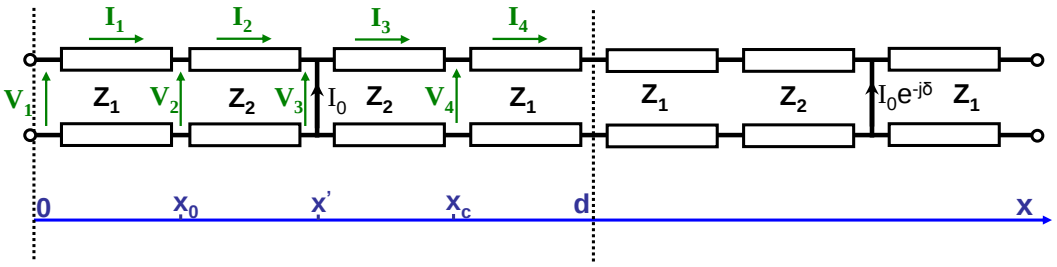

Figure A.2 Transmission line model of the feed problem of the cavity-backed patch phased array.

Appendix B: Dyadic Green's Function of the Rectangular Waveguide

In this appendix, the dyadic Green's function of the rectangular waveguide is listed as have been driven by Samii in [97] and is similar to [102].

$$\overline{\overline{G}}_e(r,r') = \overline{\overline{G}}_{eo}(r,r') - \frac{1}{k^2} z\, z\, \delta(r-r')$$

$$\overline{\overline{G}}_{eo}(r,r') = \frac{1}{k^2}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{\varepsilon_{0n}\varepsilon_{0m}}{2ab\Gamma_{nm}}\cdot e^{-\Gamma_{nm}|z-z'|}\cdot$$

$$\left\{\left(\left(\frac{m\pi}{b}\right)^2-\Gamma_{nm}^2\right)\cdot\cos\left(\frac{n\pi}{a}x\right)\cos\left(\frac{n\pi}{a}x'\right)\sin\left(\frac{m\pi}{b}y\right)\sin\left(\frac{m\pi}{b}y'\right)x\,x' + \right.$$

$$\left(\left(\frac{n\pi}{a}\right)^2-\Gamma_{nm}^2\right)\cdot\sin\left(\frac{n\pi}{a}x\right)\sin\left(\frac{n\pi}{a}x'\right)\cos\left(\frac{m\pi}{b}y\right)\cos\left(\frac{m\pi}{b}y'\right)\widehat{y\,y'} +$$

$$\left(\left(\frac{n\pi}{a}\right)^2+\left(\frac{m\pi}{b}\right)^2\right)\cdot\sin\left(\frac{n\pi}{a}x\right)\sin\left(\frac{n\pi}{a}x'\right)\cos\left(\frac{m\pi}{b}y\right)\cos\left(\frac{m\pi}{b}y'\right)\widehat{z\,z'} -$$

$$\left(\frac{n\pi}{a}\right).\left(\frac{m\pi}{b}\right)\cdot\cos\left(\frac{n\pi}{a}x\right)\sin\left(\frac{n\pi}{a}x'\right)\sin\left(\frac{m\pi}{b}y\right)\cos\left(\frac{m\pi}{b}y'\right)\widehat{x\,y'} -$$

$$\left(\frac{m\pi}{b}\right).\left(\frac{n\pi}{a}\right)\cdot\sin\left(\frac{n\pi}{a}x\right)\cos\left(\frac{n\pi}{a}x'\right)\cos\left(\frac{m\pi}{b}y\right)\sin\left(\frac{m\pi}{b}y'\right)\widehat{y\,x'} -$$

$$\left(\frac{m\pi}{b}\right).\left(\theta(z-z')-\theta(z'-z)\right)\cdot\sin\left(\frac{n\pi}{a}x\right)\sin\left(\frac{n\pi}{a}x'\right)\cos\left(\frac{m\pi}{b}y\right)\sin\left(\frac{m\pi}{b}y'\right)\widehat{y\,z'} +$$

$$\left(\frac{m\pi}{b}\right)\cdot\left(\theta(z-z')-\theta(z'-z)\right)\cdot\sin\left(\frac{n\pi}{a}x\right)\sin\left(\frac{n\pi}{a}x'\right)\sin\left(\frac{m\pi}{b}y\right)\cos\left(\frac{m\pi}{b}y'\right)\widehat{z\,y'} -$$

$$\left(\frac{n\pi}{a}\right)\cdot\left(\theta(z-z')-\theta(z'-z)\right)\cdot\cos\left(\frac{n\pi}{a}x\right)\sin\left(\frac{n\pi}{a}x'\right)\sin\left(\frac{m\pi}{b}y\right)\sin\left(\frac{m\pi}{b}y'\right)\widehat{x\,z'} +$$

$$\left.\left(\frac{n\pi}{a}\right).\left(\theta(z-z')-\theta(z'-z)\right)\cdot\sin\left(\frac{n\pi}{a}x\right)\cos\left(\frac{n\pi}{a}x'\right)\sin\left(\frac{m\pi}{b}y\right)\sin\left(\frac{m\pi}{b}y'\right)\widehat{z\,x'}\right\}$$

Where

$$\Gamma_{nm} = -k^2+\left(\frac{n\pi}{a}\right)^2+\left(\frac{m\pi}{b}\right)^2,\quad k=\omega\sqrt{\mu\varepsilon}$$

$$\varepsilon_{0m}=\begin{cases}1 & m=0\\ 2 & m\neq 0\end{cases},\quad \theta(z)=\begin{cases}1 & z>0\\ 0 & z<0\end{cases}$$

a, b are the waveguide width in x and height in y, respectively

Appendix C: Matlab Code

In this appendix, the Matlab code of the numerical analysis described in Chapter 6 is listed here.

C.1 Probe-Fed Microstrip Patch Phased Array

```
clear all

lampda0=3;
d_norm=0.52;
a_norm=0.5*d_norm;
t_norm=(d_norm-a_norm)/2;
xf_norm=a_norm/4;
xp_norm=d_norm/2+a_norm/2-xf_norm;

lampda=lampda0;

epsi_x=0;
er1=2.5;
h_norm=0.03;

Io=0.001;

C=3*10^8;
mu0=4*pi*10^-7;
epslon0=1/(C^2*mu0);

f=C/lampda;

w=2*pi*f;
k0=w/C;
z0=(mu0/(epslon0))^0.5;
z1=z0/sqrt(er1);
k1=k0*sqrt(er1);

d=d_norm*lampda0;                    % Unit cell width
t=t_norm*lampda0;                    % Slit width
a=a_norm*lampda0;                    % Patch width
xf=xf_norm*lampda0;
xp=xp_norm*lampda0;                  % Probe position
h=h_norm*lampda0;                    % Substrate thickness
s

Zo1=z1;
Zo2=z1;

xo=d/2-Wc/2;
xc=d/2+Wc/2;
```

```
step=d/1000;                          % Step size
x=[0:step:d];
xi1=0:step:t-step;
xi2=t+a+step:step:d;

N=5;                                % Total number of waveguide modes in the
moment of method basis expansion
M=6*N;

%-------------------------------------------------------------------
%      Basis Modes
%-------------------------------------------------------------------

for n=1:N
    Basis_mds1(:,n)=cos((n-1)*pi/t*xi1)./(1-(xi1/t).^2).^0.5;               %
Basis modes on A1
    Basis_mds2(:,n)=cos((n-1)*pi/(d-a-t)*(d-xi2))./(1-((d-xi2)/(d-a-
t)).^2).^0.5;   % Basis modes on A2
end

%-------------------------------------------------------------
%        Floquet Mode Expansion
%-------------------------------------------------------------

for m=1:M
        q=m-(fix(M/2)+1);
        kxm(m)=(2*pi*q+epsi_x)/d;
        Fl_mds(:,m)=((1/d)^0.5*exp(-j*kxm(m)*x));      % Floquet modes

        kz1(m)=(k1^2-kxm(m)^2)^0.5; % Floquet propagation const in the
dielectric region

        Y1(m)=(w*epslon0*er1)/kz1(m);                % Floquet modal
admittance in the dielectric region

        if k0^2>kxm(m)^2                             % Floquet propagation
const in the free space
            kz0(m)=(k0^2-kxm(m)^2)^0.5;
        else
            kz0(m)=-j*(kxm(m)^2-k0^2)^0.5;
        end

        Y0(m)=(w*epslon0)/kz0(m);                    % Floquet modal
admittance in the free space

end



for n=1:N
    for m=1:M
        f(n,m)=Probe_CosEdgeExpInt_A1(n-1,kxm(m),t,d);
```

```
    end
end

for n=1:N
    for m=1:M
        g(n,m)=Probe_CosEdgeExpInt_A2(n-1,kxm(m),t,a,d);
    end
end

fY=(Y0-j*Y1.*cot(kz1*h));
fY=diag(fY);

A1=f*fY*f';
B1=f*fY*g';
A2=g*fY*f';
B2=g*fY*g';


J1= SurfaceCurrent_ProbeFed (Io,lampda,d,xp,epsi_x,er1,xi1);
J2= SurfaceCurrent_ProbeFed (Io,lampda,d,xp,epsi_x,er1,xi2);

for n=1:N
    J_Int1(n)=simpson_int(J1.*cos((n-1)*pi/t*xi1)./(1-(xi1/t).^2).^0.5,step);
    J_Int2(n)=simpson_int(J2.*cos((n-1)*pi/(d-a-t)*(d-xi2))./(1-((d-xi2)/(d-
a-t)).^2).^0.5,step);
end

J_Int1=J_Int1.';
J_Int2=J_Int2.';

A=(A1-B1*B2^-1*A2);
an=A^-1*(J_Int1-B1*B2^-1*J_Int2);
bn=B2^-1*J_Int2-B2^-1*A2*an;

V0=f'*an+g'*bn;

Ea=Basis_mds1*an;
Eb=Basis_mds2*bn;

Ep=Fl_mds*V0;



Za_wg=-sqrt(-1)/2*h*z1*sin(k1*d)/(cos(k1*d)-cos(epsi_x));
cfl=j/(d^0.5)*kxm./kz1.^2.*exp(-j*kxm*xp);
Za_fl=1/Io*cfl*V0;
if real(Za_fl<0)
    Za_fl=-Za_fl;
end

Za=(Za_wg+Za_fl);
```

```
Ra=(real(Za));

J=SurfaceCurrent_CavityBacked(Io,lampda,d,xo,xp,xc,Zo1,Zo2,epsi_x,er1,x);

figure
plot(xi1/lampda0,abs(Ea),'b','linewidth',2.5)
hold on
plot(xi2/lampda0,abs(Eb),'b','linewidth',2.5)
plot(x/lampda0,abs(Ep),'r--','linewidth',2.5)
plot(t/lampda0.*ones(length(Ea),1),abs(Ea),'k--','linewidth',2)
plot((t+a)/lampda0.*ones(length(Ea),1),abs(Ea),'k--','linewidth',2)
grid on
ylabel('abs(Ex)','fontsize',16,'fontname','arial')
xlabel('x/lampda0','fontsize',16,'fontname','arial')
set(gca,'FontSize',16)
title(strcat('Aperture Fields, N=',num2str(N),', M=',num2str(M)))
xlim([0,d/lampda0])



function I=Probe_CosExpInt(n,k,t,d)

if n==0 & k==0
    I=(1/d)^0.5*t*pi/2;
elseif n~=0 & k==0
    I=(1/d)^0.5*t*pi/2*(besselj(0,n*pi));
elseif n==0 & k<0
    I=(1/d)^0.5*t*pi/2*(besselj(0,k*t)+j*struve0_mit(-k*t));
elseif n==0 & k>0
    I=(1/d)^0.5*t*pi/2*(besselj(0,k*t)-j*struve0_mit(k*t));
elseif (k*t-n*pi)<0 & (k*t+n*pi)<0
    I=(1/d)^0.5/2*t*pi/2*(besselj(0,k*t+n*pi)+besselj(0,k*t-n*pi)-j*(-
struve0_mit(-(k*t+n*pi))-struve0_mit(-(k*t-n*pi))));
elseif (k*t-n*pi)>0 & (k*t+n*pi)<0
    I=(1/d)^0.5/2*t*pi/2*(besselj(0,k*t+n*pi)+besselj(0,k*t-n*pi)-j*(-
struve0_mit(-(k*t+n*pi))+struve0_mit((k*t-n*pi))));
elseif (k*t-n*pi)<0 & (k*t+n*pi)>0
    I=(1/d)^0.5/2*t*pi/2*(besselj(0,k*t+n*pi)+besselj(0,k*t-n*pi)-
j*(struve0_mit(k*t+n*pi)-struve0_mit(-(k*t-n*pi))));
else
    I=(1/d)^0.5/2*t*pi/2*(besselj(0,k*t+n*pi)+besselj(0,k*t-n*pi)-
j*(struve0_mit(k*t+n*pi)+struve0_mit(k*t-n*pi)));
end
```

```
function I=Probe_CosExpInt(n,k,t,a,d)

if n==0 & k==0
   I=(1/d)^0.5*(d-a-t)*pi/2;
elseif n~=0 & k==0
   I=(1/d)^0.5*(d-a-t)*pi/2*(besselj(0,n*pi));
elseif n==0 & k<0
   I=exp(-j*k*d)*(1/d)^0.5*(d-a-t)*pi/2*(besselj(0,k*(d-a-t))-j*struve0_mit(-
k*(d-a-t)));
elseif n==0 & k>0
   I=exp(-j*k*d)*(1/d)^0.5*(d-a-t)*pi/2*(besselj(0,k*(d-a-
t))+j*struve0_mit(k*(d-a-t)));
elseif (k*(d-a-t)-n*pi)<0 & (k*(d-a-t)+n*pi)<0
   I=exp(-j*k*d)*(1/d)^0.5/2*(d-a-t)*pi/2*(besselj(0,k*(d-a-
t)+n*pi)+besselj(0,k*(d-a-t)-n*pi)+j*(-struve0_mit(-(k*(d-a-t)+n*pi))-
struve0_mit(-(k*(d-a-t)-n*pi))));
elseif (k*(d-a-t)-n*pi)>0 & (k*(d-a-t)+n*pi)<0
   I=exp(-j*k*d)*(1/d)^0.5/2*(d-a-t)*pi/2*(besselj(0,k*(d-a-
t)+n*pi)+besselj(0,k*(d-a-t)-n*pi)+j*(-struve0_mit(-(k*(d-a-
t)+n*pi))+struve0_mit((k*(d-a-t)-n*pi))));
elseif (k*(d-a-t)-n*pi)<0 & (k*(d-a-t)+n*pi)>0
   I=exp(-j*k*d)*(1/d)^0.5/2*(d-a-t)*pi/2*(besselj(0,k*(d-a-
t)+n*pi)+besselj(0,k*(d-a-t)-n*pi)+j*(struve0_mit(k*(d-a-t)+n*pi)-
struve0_mit(-(k*(d-a-t)-n*pi))));
else
   I=exp(-j*k*d)*(1/d)^0.5/2*(d-a-t)*pi/2*(besselj(0,k*(d-a-
t)+n*pi)+besselj(0,k*(d-a-t)-n*pi)+j*(struve0_mit(k*(d-a-
t)+n*pi)+struve0_mit(k*(d-a-t)-n*pi)));
end



function [J,v,c]=SurfaceCurrent_ProbeFed(Io,lampda0,d,xp,delta,er1,xi)

c0=2.998*10^8;
mu0=4*pi*10^-7;
epslon0=1/(c0^2*mu0);

f=c0/lampda0;
w=2*pi*f;
k0=w/c0;
k=k0*sqrt(er1);

z0=(mu0/(epslon0))^0.5;
Z1=z0/(er1)^0.5;


v1p=[ -1/2*exp(-i*(k*d-k*xp-delta))/(exp(-i*(k*d-delta))-1)*Io*Z1];
v1n=[    1/2*exp(i*(k*d-k*xp+delta))/(exp(i*(k*d+delta))-1)*Io*Z1];
v2p=[                           -1/2/(exp(-i*(k*d-delta))-1)*Io*Z1];
v2n=[                             1/2/(exp(i*(k*d+delta))-1)*Io*Z1];
```

```
x=xi;

for n=1:length(x)
    if x(n)>=0 & x(n)<xp
        I(n)=v1p/Z1*exp(-j*k*x(n))-v1n/Z1*exp(j*k*x(n));
    elseif x(n)>=xp & x(n)<=d
        I(n)=v2p/Z1*exp(-j*k*(x(n)-xp))-v2n/Z1*exp(j*k*(x(n)-xp));
    end
end

v=[v1p v1n v2p v2n];
c=[exp(-j*k*(x-xp)).' exp(j*k*(x-xp)).'];
J=-I;
```

C.2 Probe-Fed Cavity-Backed Patch Phased Array (Case of Two Substrates)

```
clear all

c0=299792458 ;
lampda0=3;
lampda=3;
d_norm=0.51;
a_norm=0.25;
xf_norm=0;

theta=0;
theta=theta/180*pi;

er1=2.2;
h_norm=0.01;
hc_norm=0.12;
Wc_norm=0.42;



c=299792458 ;
mu0=4*pi*10^-7;
epslon0=1/(c^2*mu0);

f=c/lampda;
w=2*pi*f;
k0=w/c;
z0=(mu0/(epslon0))^0.5;
z1=z0/(er1)^0.5;
k1=k0*sqrt(er1);

d=d_norm*lampda0;                    % Unit cell width
a=a_norm*lampda0;                    % Patch width
t=(d-a)/2;                           % Slit width
xf=xf_norm*lampda0;
xp=d/2+a/2-xf;                       % Probe position
h=h_norm*lampda0;                    % Substrate thickness
Wc=Wc_norm*lampda0;
hc=hc_norm*lampda0;

epsi_x=2*pi/lampda0*d*sin(theta);

lampdaN=3;
Normfactor=lampdaN/lampda;

Io=0.001;


mu0=4*pi*10^-7;
epslon0=1/(c^2*mu0);
```

```
f=c/lampda;
w=2*pi*f;
k0=w/c;
z0=(mu0/(epslon0))^0.5;
z1=z0/(er1)^0.5;
k1=k0*sqrt(er1);

Zo1=z1*h;
Zo2=z1*(h+hc);

xo=d/2-Wc/2;
xc=d/2+Wc/2;

step=d/1000;                          % Step size
x=[0:step:d];                          %
xi1=0:step:t-step;
xi2=t+a+step:step:d;
xic=xo:step:xc;
% Equivalent h
N=5;             % Total number of basis modes
Ng=N;            % Total number of waveguide modes
M=20*N;             % Total number of Floquet modes


%---------------------------------------------------------------------
%      Basis Modes
%---------------------------------------------------------------------

for n=1:N
    Basis_mds1(:,n)=cos((n-1)*pi/t*xi1)./(1-(xi1/t).^2).^0.5;                %
Basis modes on A1
    Basis_mds2(:,n)=cos((n-1)*pi/(d-a-t)*(d-xi2))./(1-((d-xi2)/(d-a-
t)).^2).^0.5;    % Basis modes on A2
end

%---------------------------------------------------------------------
%      Wg Modes
%---------------------------------------------------------------------

for n=1:Ng
    Wg_mds(:,n)=sqrt(2/Wc)*cos((n-1)*pi/Wc*(xic-xo));          % Basis modes
    kxg(n)=((n-1)*pi)/Wc;
    Bgz(n)=(k1^2-kxg(n)^2)^0.5;
    yg(n)=(w*epslon0*er1)/Bgz(n);
end

%---------------------------------------------------------------
%        Floquet Mode Expansion
%---------------------------------------------------------------

for m=1:M
        q=m-(fix(M/2)+1);
        kxm(m)=(2*pi*q+epsi_x)/d;
        Fl_mds(:,m)=((1/d)^0.5*exp(-j*kxm(m)*x));       % Floquet modes
```

```
      kz1(m)=(k1^2-kxm(m)^2)^0.5; % Floquet propagation const in the
      dielectric


        Y1(m)=(w*epslon0*er1)/kz1(m);                    % Floquet modal
admittance in the dielectric region

        if k0^2>kxm(m)^2                                 % Floquet propagation
const in the free space
            kz0(m)=(k0^2-kxm(m)^2)^0.5;
        else
            kz0(m)=-j*(kxm(m)^2-k0^2)^0.5;
        end

        Y0(m)=(w*epslon0)/kz0(m);                        % Floquet modal
admittance in the free space

end


for n=1:Ng
    for m=1:M
        C(n,m)=Probe_CosExpInt_Wc(n-1,kxm(m),xo,xc,Wc,d);
    end
end

for n=1:N
    for m=1:M
        f(n,m)=Probe_CosEdgeExpInt_A1(n-1,kxm(m),t,d);
    end
end

for n=1:N
    for m=1:M
        g(n,m)=Probe_CosEdgeExpInt_A2(n-1,kxm(m),t,a,d);
    end
end


fyg=sqrt(-1)*(1./yg).*(1./(cot(Bgz*hc)));

B=diag(Y1)*C'*diag(fyg)*C;

B=B.';

I=eye(M,M);

S=(I-B)^-1*(I+B);

P=diag(exp(-sqrt(-1)*kz1*h))-S*diag(exp(sqrt(-1)*kz1*h));
```

```
Q=diag(exp(-sqrt(-1)*kz1*h))+S*diag(exp(sqrt(-1)*kz1*h));


R=(diag(Y0)-diag(Y1)*P^-1*Q);

A1=f*R*f';
B1=f*R*g';
A2=g*R*f';
B2=g*R*g';

J=SurfaceCurrent_CavityBacked(Io,lampda,d,xo,xp,xc,Zo1,Zo2,epsi_x,er1,x);

for n=1:N
     J_Int1(n)=quadgk(@(xi)CurrentEdgeBasis_A1(xi,n-
1,t,d,Io,lampda,xo,xp,xc,Zo1,Zo2,epsi_x,er1),0,t);
     J_Int2(n)=quadgk(@(xi)CurrentEdgeBasis_A2(xi,n-
1,t,a,d,Io,lampda,xo,xp,xc,Zo1,Zo2,epsi_x,er1),t+a,d);
end

J_Int1=J_Int1.';
J_Int2=J_Int2.';

A=(A1-B1*B2^-1*A2);
an=A^-1*(J_Int1-B1*B2^-1*J_Int2);
bn=B2^-1*(J_Int2-A2*an);

V0=f'*an+g'*bn;

Vp=P^-1*V0;
Vn=-S*Vp;

for n=1:Ng
    v(n)=-fyg(n)*Y1.*C(n,:)*(Vp-Vn);
end

v=v.';

% Check
VcheckP=Vp+Vn;
VcheckN=C'*v;
norm(VcheckP)
norm(VcheckN)

Vcheck1=Vp.*exp(-sqrt(-1)*kz1.'*h)+Vn.*exp(sqrt(-1)*kz1.'*h);
norm(V0)
norm(Vcheck1)


%--------------------------------------------------------------------
% Active Impedance
```

```
Vc=SurfaceCurrent_CavityBacked_v(Io,lampda,d,xo,xp,xc,Zo1,Zo2,epsi_x,er1,xp);
V1p=Vc(1);
V1n=Vc(2);
V2p=Vc(3);
V2n=Vc(4);
V3p=Vc(5);
V3n=Vc(6);
V4p=Vc(7);
V4n=Vc(8);

Za_wg=-(V3p+V3n)/Io*(h+hc);

cg=(sqrt(2/Wc).*kxg./Bgz.^2.*sin(kxg*(xp-xo)));
Za_cavity=1/Io*cg*v;

norm_v=norm(v)
norm_cg=norm(cg)

cfl=2/sqrt(d)*kxm./kz1.^2.*exp(-sqrt(-1)*kxm*xp).*sin(kz1*h/2);
cp=exp(-sqrt(-1)*kz1*h/2);
cn=exp(sqrt(-1)*kz1*h/2);
cflp=cfl.*cp;
cfln=cfl.*cn;

norm_cflp=norm(cflp)
norm_Vp=norm(Vp)
norm_cfln=norm(cfln)
norm_Vn=norm(Vn)

Za_fl=1/Io*(cflp*Vp-cfln*Vn);

Za=(Za_fl+Za_wg+Za_cavity)*Normfactor;

if real(Za)<0
    Za=-Za;
end

Za_wg
Za_cavity
Za_fl
Za

%-------------------------------------------------
Ea=Basis_mds1*an;
Eb=Basis_mds2*bn;

E0=Fl_mds*V0;
E1=Fl_mds*(Vp.*exp(-sqrt(-1)*kz1.'*h)+Vn.*exp(sqrt(-1)*kz1.'*h));

Ed=Fl_mds*(Vp+Vn);
Eg=Wg_mds*v;

figure
```

```
plot(x/lampda0,abs(J),'b','linewidth',2)
hold on
grid on
plot(xp/lampda0.*ones(length(J),1),abs(J),'r--','linewidth',2)
plot(t/lampda0.*ones(length(J),1),abs(J),'k--','linewidth',2)
plot((t+a)/lampda0.*ones(length(J),1),abs(J),'k--','linewidth',2)
plot(xo/lampda0.*ones(length(J),1),abs(J),'m--','linewidth',2)
plot(xc/lampda0.*ones(length(J),1),abs(J),'m--','linewidth',2)
ylabel('abs(J)','fontsize',16,'fontname','arial')
xlabel('x/lampda0','fontsize',16,'fontname','arial')
set(gca,'FontSize',16)
xlim([0/lampda0,d/lampda0])

figure
plot(xi1/lampda0,abs(Ea),'b','linewidth',2)
hold on
plot(xi2/lampda0,abs(Eb),'b','linewidth',2)
plot(x/lampda0,abs(E1),'m--','linewidth',2)
plot(x/lampda0,abs(E0),'r:','linewidth',2)
plot(t/lampda0.*ones(length(Eb),1),abs(Eb),'k--','linewidth',2)
plot((t+a)/lampda0.*ones(length(Eb),1),abs(Eb),'k--','linewidth',2)
grid on
ylabel('abs(Ex)','fontsize',16,'fontname','arial')
xlabel('x','fontsize',16,'fontname','arial')
set(gca,'FontSize',16)
xlim([0/lampda0,d/lampda0])
title(strcat('Aperture Fields at Z=hs, N=',num2str(N),', M=',num2str(M)))
legend('E-Ap-L','E-Ap-R','E-Fl-D','E-Fl-Air')

figure
plot(xic/lampda0,abs(Eg),'b','linewidth',2)
hold on
plot(x/lampda0,abs(Ed),'r:','linewidth',2)
grid on
plot(xo/lampda0.*ones(length(Eg),1),abs(Eg),'k--','linewidth',2)
plot(xc/lampda0.*ones(length(Eg),1),abs(Eg),'k--','linewidth',2)

ylabel('abs(Ex)','fontsize',16,'fontname','arial')
xlabel('x','fontsize',16,'fontname','arial')
set(gca,'FontSize',16)
xlim([0/lampda0,d/lampda0])
title(strcat('Aperture Fields at Z=0, Ng=',num2str(Ng),', M=',num2str(M)))
legend('E-guide','E-Fl-D')

function I=Probe_CosExpInt_Wc(n,k,xo,xc,Wc,d)

if n==0 & k==0
    I=(1/d)^0.5*(1/Wc)^0.5*Wc;
elseif n~=0 & k==0
    I=0;
else
    I=(1/d)^0.5*(2/Wc)^0.5*(-Wc*(-j*k*Wc+j*k*Wc*exp(-
j*k*xc+xo*j*k)*cos(n*pi*(xo-xc)/Wc)+n*pi*exp(-j*k*xc+xo*j*k)*sin(n*pi*(xo-
xc)/Wc))*exp(-xo*j*k)/(j^2*k^2*Wc^2+n^2*pi^2));
end
```

C.3 Probe-Fed Cavity-Backed Patch Phased Array (Case of Single Substrate)

```
clear all


c0=299792458 ;
mu0=4*pi*10^-7;
epslon0=1/(c0^2*mu0);

f0=10e9;
lampda0=c0/f0;

f=10e9;
lampda=c0/f;

theta=0.001;
theta=theta/180*pi;
er=2.2;

d_norm=0.5;
a_norm=0.27;
hc_norm=0.1;
Wc_norm=0.4;
xf=a_norm/15;


d=d_norm*lampda0;                    % Unit cell width
a=a_norm*lampda0;                    % Patch width
hc=hc_norm*lampda0;                  % Substrate/Cavity thickness
Wc=Wc_norm*lampda0;
xf=xf*lampda0;
xa1=d/2-a/2;
xa2=d/2+a/2;
xo=d/2-Wc/2;
xc=d/2+Wc/2;
xp=xa2-xf;                         % Probe position
t=xa1-xo;

epsi_x=2*pi/lampda0*d*sin(theta);

f=c0/lampda;
w=2*pi*f;
k0=w/c0;
k1=k0*sqrt(er);

step=d/1000;                        % Step size
x=[0:step:d];                        %
xi1=xo+step/10:step:xa1;
xi2=xa2+step/10:step:xc-step/10;
xic=xo:step:xc;
xip=xa1:step:xa2;
```

```
N=3;             % Total number of basis modes
Ng=5*N+1;          % Total number of waveguide modes
M=5*N+1;          % Total number of Floquet modes

Nx=5;            % Total number of modes in x for the feed problem
Mz=1;            % Total number of modes in z for the feed problem

%--------------------------------------------------------------------
%      Basis Modes
%--------------------------------------------------------------------
for n=1:N
    Basis_mds1(:,n)=cos((n-1)*pi/t*(xi1-xo))./(1-((xi1-xo)/t).^2).^0.5;
% Basis modes on A1
    Basis_mds2(:,n)=cos((n-1)*pi/t*(xc-xi2))./(1-((xc-xi2)/t).^2).^0.5;    %
Basis modes on A2
end
%--------------------------------------------------------------------
%      Wg Modes
%--------------------------------------------------------------------
for n=1:Ng
    Wg_mds(:,n)=sqrt(2/Wc)*cos((n-1)*pi/Wc*(xic-xo)); % Wg modes
    kxg(n)=((n-1)*pi)/Wc;
    if k1^2>kxg(n)^2                                  % propagation const in
the dielectric region
        Bgz(n)=(k1^2-kxg(n)^2)^0.5;
    else
        Bgz(n)=-sqrt(-1)*(kxg(n)^2-k1^2)^0.5;
    end
    yg(n)=(w*epslon0*er)/Bgz(n);
end
%-------------------------------------------------------------
%        Floquet Mode Expansion
%-------------------------------------------------------------
for m=1:M
        q=m-(fix(M/2)+1);
        kxm(m)=(2*pi*q+epsi_x)/d;
        Fl_mds(:,m)=((1/d)^0.5*exp(-sqrt(-1)*kxm(m)*x));      % Floquet modes
        if k0^2>kxm(m)^2                                   % Floquet propagation
const in the free space
            kz0(m)=(k0^2-kxm(m)^2)^0.5;
        else
            kz0(m)=-sqrt(-1)*(kxm(m)^2-k0^2)^0.5;
        end
        Y0(m)=(w*epslon0)/kz0(m);                          % Floquet modal
admittance in the free space
end
%-------------------------------------------------------------
%        Intermodal coupling coefficients
%-------------------------------------------------------------

for n=1:Ng
    for m=1:M
        C(n,m)=quadgk(@(xi)GroveWgmdsFlmds(xi,xo,n-1,Wc,kxm(m),d),xo,xc);
    end
end
```

```
for n=1:M
    for m=1:N
        f1(m,n)=quadgk(@(xi)GroveFlmdsEdgeBasis_A1(xi,kxm(n),d,m-
1,xo,t),xo,xa1);
        f2(m,n)=quadgk(@(xi)GroveFlmdsEdgeBasis_A2(xi,kxm(n),d,m-
1,t,xc),xa2,xc);
    end
end

for n=1:N
    for m=1:Ng
        g1(n,m)=quadgk(@(xi)GroveWgmdsEdgeBasis_A1(xi,xo,n-1,Wc,m-
1,t),xo,xa1);
        g2(n,m)=quadgk(@(xi)GroveWgmdsEdgeBasis_A2(xi,xo,n-1,Wc,m-
1,t,xc),xa2,xc);
    end
end

Yg=sqrt(-1)*(yg).*cot(Bgz*hc);

A1=f1*diag(Y0)*f1'-g1*diag(Yg)*(C*C')^-1*C*f1';
B1=f1*diag(Y0)*f2'-g1*diag(Yg)*(C*C')^-1*C*f2';
A2=f2*diag(Y0)*f1'-g2*diag(Yg)*(C*C')^-1*C*f1';
B2=f2*diag(Y0)*f2'-g2*diag(Yg)*(C*C')^-1*C*f2';

Js1=SurfaceCurrent_GroveBacked(lampda0,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz,xi1);
Js2=SurfaceCurrent_GroveBacked(lampda0,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz,xi2);

Js_patch=SurfaceCurrent_GroveBacked(lampda0,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz,xip)
;

for n=1:N
     J_Int1(n)=quadgk(@(xi)GroveCurrentEdgeBasis_A1(xi,n-
1,xo,t,lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz),xo,xa1);
     J_Int2(n)=quadgk(@(xi)GroveCurrentEdgeBasis_A2(xi,n-
1,t,xc,lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz),xa2,xc);
end

J_Int1=-J_Int1.';
J_Int2=-J_Int2.';

A=(A1-B1*B2^-1*A2);
an=A^-1*(J_Int1-B1*B2^-1*J_Int2);
bn=B2^-1*(J_Int2-A2*an);

V0=f1'*an+f2'*bn;

v=(C*C')^-1*C*V0;

% Check
VcheckP=V0;
VcheckN=C'*v;
```

```
norm(VcheckP)
norm(VcheckN)

Zaf=ZaFeed_GroveBacked(lampda,d,a,Wc,hc,xf,er,epsi_x,Nx);

Zar=-1/(sqrt(-1)*w*epslon0*er)*sqrt(2/Wc)*yg./Bgz.*kxg.*sin(kxg*(xp-xo))*v;

dp=1/3;

Za=(Zaf+Zar)/dp

%-------------------------------------------------
Ea=Basis_mds1*an;
Eb=Basis_mds2*bn;

E0=Fl_mds*V0;
Eg=Wg_mds*v;

figure
plot(xi1/lampda0,abs(Ea)/1000,'b','linewidth',2)
hold on
plot(xi2/lampda0,abs(Eb)/1000,'b','linewidth',2)


plot(xic/lampda0,abs(Eg)/1000,'r--','linewidth',2)

plot(xo/lampda0.*ones(length(Ea),1),abs(Ea)/1000,'k--','linewidth',2)
plot(xa1/lampda0.*ones(length(Ea),1),abs(Ea)/1000,'k--','linewidth',2)
plot(xa2/lampda0.*ones(length(Ea),1),abs(Ea)/1000,'k--','linewidth',2)
plot(xc/lampda0.*ones(length(Ea),1),abs(Ea)/1000,'k--','linewidth',2)

grid on
ylabel('abs(Ex)','fontsize',16,'fontname','arial')
xlabel('x/lambda0','fontsize',16,'fontname','arial')
set(gca,'FontSize',16)
xlim([0/lampda0,d/lampda0])
legend('E-Ap-L','E-Ap-R','E-G')
ylim([0 1e2])

figure
plot(xi1/lampda0,abs(Js1),'b','linewidth',2)
hold on
plot(xi2/lampda0,abs(Js2),'b','linewidth',2)
plot(xip/lampda0,abs(Js_patch),'r','linewidth',2)
plot(xo/lampda0.*ones(length(Js1),1),abs(Js1),'k--','linewidth',2)
plot(xa1/lampda0.*ones(length(Js1),1),abs(Js1),'k--','linewidth',2)
plot(xa2/lampda0.*ones(length(Js1),1),abs(Js1),'k--','linewidth',2)
plot(xc/lampda0.*ones(length(Js1),1),abs(Js1),'k--','linewidth',2)
grid on
ylabel('abs(Js)','fontsize',16,'fontname','arial')
xlabel('x','fontsize',16,'fontname','arial')
set(gca,'FontSize',16)
xlim([0/lampda0,d/lampda0])
```

```
set(gca,'FontSize',16)


function y=GroveWgmdsFlmds(x,xo,n,Wc,kx,d)
y=GroveWgMds(x,xo,n,Wc).*GroveFlMds(x,kx,d);

function y=GroveFlmdsEdgeBasis_A1(x,kx,d,m,xo,t)
y=GroveFlMds(x,kx,d).*GroveBasisEdge_A1(x,m,xo,t);


function y=GroveFlmdsEdgeBasis_A2(x,kx,d,m,t,xc)
y=GroveFlMds(x,kx,d).*GroveBasisEdge_A2(x,m,t,xc);


function y=GroveWgmdsEdgeBasis_A1(x,xo,n,Wc,m,t)
y=GroveWgMds(x,xo,n,Wc).*GroveBasisEdge_A1(x,m,xo,t);


function y=GroveWgmdsEdgeBasis_A2(x,xo,n,Wc,m,t,xc)
y=GroveWgMds(x,xo,n,Wc).*GroveBasisEdge_A2(x,m,t,xc);


function y=GroveWgMds_A1(x,xo,n,Wc)
y=sqrt(2/Wc)*cos(n*pi/Wc*(x-xo));


function y=GroveFlMds(x,kx,d)
y=sqrt(1/d)*exp(-sqrt(-1)*kx*x);


function y=GroveBasisEdge_A1(x,n,xo,t)
y=cos(n*pi/t*(x-xo))./(1-((x-xo)/t).^2).^0.5;


function y=GroveBasisEdge_A2(x,n,t,xc)
y=cos(n*pi/(t)*(xc-x))./(1-((xc-x)/t).^2).^0.5;

function
y=GroveCurrentEdgeBasis_A1(x,n,xo,t,lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz)
y=SurfaceCurrent_GroveBacked(lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz,x).*GroveBas
isEdge_A1(x,n,xo,t);

function
y=GroveCurrentEdgeBasis_A2(x,n,t,xc,lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz)
y=SurfaceCurrent_GroveBacked(lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz,x).*GroveBas
isEdge_A2(x,n,t,xc);


function
Jsx=SurfaceCurrent_GroveBacked(lampda,d,a,Wc,hc,xf,er,epsi_x,Nx,Mz,x)


c0=2.998*10^8;
mu0=4*pi*10^-7;
epslon0=1/(c0^2*mu0);

f=c0/lampda;
```

```
w=2*pi*f;
k0=w/c0;
k=k0*sqrt(er);

xa1=d/2-a/2;                    % Patch Start Point
xa2=d/2+a/2;                    % Patch End Point
xo=d/2-Wc/2;                    % Cavity Start Point
xc=d/2+Wc/2;                    % Cavity End Point
xp=xa2-xf;                      % Probe Location w.r.t. origin

%-----------------------------------------------------------------
%      Feed Problem
%-----------------------------------------------------------------
  %Nx=4;          % number of modes in x
  n=0:1:Nx-1;
  e0n=2*ones(1,Nx);
  e0n(1)=1;

  %Mz=2;          % number of modes in z
  m=0:1:Mz-1;
  e0m=2*ones(1,Mz);
  e0m(1)=1;


  kx=n*pi/Wc;
  kz=m*pi/hc;

  for i=1:length(n)
      for j=1:length(m)
          if (kx(i)^2+kz(j)^2)>k^2
            Gamma(i,j)=sqrt(kx(i)^2+kz(j)^2-k^2);
          else
            Gamma(i,j)=-sqrt(-1)*sqrt(k^2-kx(i)^2-kz(j)^2);
          end
          Sm(i,j)=e0n(i)*hc/(4*Wc*Gamma(i,j))*(kx(i)^2-
Gamma(i,j)^2)*sin(kx(i)*(xp-xo))^2;
      end
  end

  Sm=sum(Sm);
  Im=k^2/(sqrt(-1)*w)*1./Sm;


   for i=1:length(n)
       for j=1:length(m)
            Jsnm(:,i,j)=-1/mu0*e0n(i)*e0m(j)*kx(i)/(4*Wc*Gamma(i,j))*Im(j)*(-
1)^j*sin(kx(i)*(xp-xo)).*cos(kx(i)*(x-xo));
       end
   end

   Jsx=exp(-sqrt(-1)*epsi_x)*sum(sum(Jsnm,3),2).';
```

```
function Zaf=ZaFeed_GroveBacked(lampda0,d,a,Wc,hc,xf,er,epsi_x,Nx)


c0=2.998*10^8;
mu0=4*pi*10^-7;
epslon0=1/(c0^2*mu0);

f=c0/lampda0;
w=2*pi*f;
k0=w/c0;
k=k0*sqrt(er);

xa1=d/2-a/2;                    % Patch Start Point
xa2=d/2+a/2;                    % Patch End Point
xo=d/2-Wc/2;                    % Cavity Start Point
xc=d/2+Wc/2;                    % Cavity End Point
xp=xa2-xf;                      % Probe Location w.r.t. origin

%-----------------------------------------------------------------
%      Feed Problem
%-----------------------------------------------------------------
  %Nx=4;          % number of modes in x
  n=0:1:Nx;
  e0n=2*ones(1,Nx+1);
  e0n(1)=1;

  %Mz=2;          % number of modes in z
  m=0;
  e0m(1)=1;

  kx=n*pi/Wc;
  kz=m*pi/hc;

  for i=1:length(n)
      for j=1:length(m)
          Gamma(i,j)=sqrt(kx(i)^2+kz(j).^2-k^2);
          Sm(i,j)=e0n(i)*e0m(j)*hc/(8*Wc*Gamma(i,j))*(kx(i)^2-
Gamma(i,j)^2)*sin(kx(i)*(xp-xo))^2;
      end
  end

  Sm=sum(Sm);
  Im=1/(sqrt(-1)*w)*1./Sm;


   for i=1:length(n)
       Zafn=sqrt(-1)*w*e0n(i)/(4*Wc*Gamma(i,1))*(kx(i)^2-
Gamma(i,1)^2)*sin(kx(i)*(xp-xo))^2*Im*hc;
   end

Zaf=exp(-sqrt(-1)*epsi_x)*sum(Zafn);
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Vita

Mohamed Awida received the B.Sc. and M.Sc. in electrical engineering from Ain Shams University, Cairo, Egypt in 2002, 2006, respectively. He has been a research and teaching assistant at Ain Shams University from 2002 to 2006. In summer 2005, he was a visiting scholar in Otto-Von-Guericke University, Magdeburg, Germany. In Aug. 2006, he joined the University of Tennessee at Knoxville where he worked towards the Ph.D. degree. From Oct. 2008 to May 2009, he was a research assistant in the Spallation Neutron Source, Oak Ridge National Lab. His research interests include antenna arrays for mobile platforms, microwave passive planar structures, and microwave linear particle accelerators.

Mr. Awida is listed in Who's Who in the World 2006 and is a member of Phi Kappa Phi honor society. In Dec 2010, he received the Bardeen Fellowship from Fermi National Lab where is working as superconducting RF engineer.